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Silicon Non-blocking 4×4 Optical Switch Chip Integrated With Both Thermal and Electro-optic Tuners

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Abstract: We experimentally demonstrate an integrated strictly non-blocking silicon 4×4 optical switch chip that can be operated in both thermo-optic (TO) and electro-optic (EO) switching modes. It is based on the double-layer network (DLN) architecture and consists of twelve 2×2 Mach-Zehnder interferometer (MZI) switch elements. TO phase shifters based on TiN microheaters and EO phase shifters based on p-i-n diodes are embedded in both waveguide arms of the MZI elements. The power consumption for TO and EO switching is 34 mW/π and 7 mW/π, respectively. The on-chip insertion losses are 1.74 ± 0.59 dB and 3.79 dB ± 1.32 dB for TO and EO switching, respectively. Due to the merits of the DLN architecture and the optimized performance of the switch elements, the chip possesses low crosstalk of -29.1 dB and -19.4 dB for TO and EO switching, respectively. Quadrature phase-shift keying (QPSK) optical signals with a data rate of 64 Gb/s are transmitted through the switch with no observable deteriorations. Such an optical switch is a promising candidate for both optical circuit switching and optical packet switching for a variety of applications.

Index Terms: Silicon nanophotonics, waveguide devices, integrated nanophotonic systems.

1. Introduction

Integrated large-port-count optical switches are highly demanded to enable sustainable growth of diverse optical transmission networks from long-haul to short-reach distance scales, which can greatly expand network bandwidth and reduce electrical power consumption [1-3]. In short-reach networks, optical switches bypass the pin and power limitations imposed by electronic switches and also simplify the whole systems by eliminating the costly and inefficient opto-electronic and electro-optic conversions [4]. In long-haul networks, integrated optical switches are also satisfactory for lowering the cost over current switching technologies. Silicon photonics has the advantages of compact size due to its large refractive index contrast, and low cost for the complementary metal-oxide-semiconductor (CMOS) compatible manufacturing processes, which are favorable for large-scale optical switches. Various silicon optical switch metrics with different actuation methods and switch elements have been demonstrated, such as micro-electro-mechanical system (MEMS) actuated crossbar switches [5-7], thermo-optic (TO) Mach-Zehnder interferometer (MZI) switches [8-11], TO micro-ring based switches [12-15], electro-optic (EO) MZI switches [16-19], EO dual-ring-assisted MZI switches [20, 21], etc. Typically, the switching speed of MEMS and TO based optical switches is in the order of microseconds, while EO actuated switches based on the free-carrier dispersion effect have a faster response time of nanoseconds. Optical switches with microsecond and nanosecond reconfiguration time are both required for various applications. For example, in data center applications, hybrid networks composed of optical-circuit/electrical-packet switching are proposed by researchers. The optical circuit switching is used to handle the more diverse workload and exist closer to the end hosts, in which microsecond-scale reconfiguration time is required [22]. However, in data-intensive workloads, where switching is operated at a packet granularity with typically less than 20 ns packet durations, reconfiguration time on the order of nanoseconds or less are preferred. In multi-plane or multi-path networks or for applications that allow longer messages, switching time on the order of tens of nanoseconds could also be tolerated [3].

However, most of the proposed optical switches are demonstrated with only one switching actuator. Although several reported optical switches are integrated with both TO and EO phase shifters in the chip, the TO phase shifters are just used for phase compensation from fabrication errors [17, 21, 23]. It still brings extra loss due to EO switching, which is not the optimal solution for the applications like optical-circuit switching. In this work, we experimentally demonstrate a silicon 4×4 strictly non-blocking optical switch chip that can be operated in both TO and EO modes. We characterize the switching performance of all the 24 switching states for both TO and EO switching, which shows on-chip insertion loss of 1.74 ± 0.59 dB and 3.79 dB ± 1.32 dB upon TO and EO switching, respectively. The crosstalk is better than -29.1 dB and -19.4 dB for TO and EO tuning, respectively. High-speed data transmission experiments are also performed to verify the routing capability of the proposed switch. Such a silicon optical switch chip capable of switching in both microsecond and nanosecond response times has wider and more flexible applications in various fields. The operation mode can be easily switched according to the practical requirements.

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2. Device structure and implementation

2.1. Switch architecture

The switch is based on the double-layer network (DLN) architecture, as shown in Fig. 1(a). The input and output ports are defined as I_m and O_m (m = 1, 2, …, N). The DLN is a strictly non-blocking architecture, first proposed by Lu and Thompson [24]. It consists of three logical stages. For an $N\times N$ DLN switch, the left- and right-end stages both own N switch elements, which work as 1×2 switches and 2×1 switches, respectively. The middle stage has four $N/2\times N/2$ subnetworks. Logically, a DLN is separated into two layers, namely "upper" and "lower" layers. Each layer consists of two stages of $N/2$ switch elements and two $N/2\times N/2$ subnetworks. In the left-end stage, the $N/2$ elements in the upper layer connect to the first and third subnetworks, while the $N/2$ elements in the lower layer connect to the second and fourth subnetworks. In the right-end stage, the $N/2$ elements in the upper layer connect to the first and second subnetworks, while the $N/2$ elements in the lower layer connect to the third and fourth subnetworks. The $N/2\times N/2$ subnetworks are constructed recursively until reach 2×2 switch networks. A 2×2 DLN can be just a simple 2×2 switch element.

The routing algorithm for the DLN matrix is also simple and recursive. For a switching path I_i-O_j (i, j = 1, 2, …, N), the i^{th} and j^{th} switch elements in the left and right stages are routed to the first subnetwork if $i \le N/2$, $j \le N/2$. Otherwise, when $i \le N/2$, $j > N/2$, these two elements are routed to the third subnetwork. If the input ports are in the lower layer ($i > N/2$), the i^{th} and j^{th} elements of the two outer stages are connected to the second ($j \le N/2$) and the fourth ($j > N/2$) subnetwork, respectively. Therefore, each connection has its own fixed routing path, and therefore, the DLN is strictly non-blocking.

The total number of switch elements required for an $N\times N$ DLN switch is $(5/4)N^2$-$2N$. In each switching path, there are $2\log_2(N)$-1 switch elements (same as the Benes switch), which is much less than the N switch elements in the PILOSS switch. The maximum number of waveguide crossings in paths is in the order of O(N), less than the O(N^2) of the switch-and-select switches. Besides, the DLN is immune to the first-order crosstalk, except for the middle stage. The DLN is also impervious to multipath interference, which potentially gives lower crosstalk than the Benes and PILOSS fabrics. Another well-known switch architecture is the dilated Banyan topology. It uses one more stage of switch elements in the middle to completely cancel the first order crosstalk in the expense of a slightly higher insertion loss and a larger footprint. Therefore, the DLN architecture has balanced loss and crosstalk performance in comparison with the Benes, PILOSS, switch-and-select architectures, dilated Banyan, which is suitable for large-port-count silicon optical switches [25]. The shortage for the DLN switch fabric is the large footprint, as the number of switch elements grows as O(N^2). Fig. 1(b) shows the schematic of a 4×4 DLN switch, composed of 12 switch elements. The elements in the i^{th} row and j^{th} column is defined as Mij (i=1, 2, 3, and j=1, 2, 3, 4).

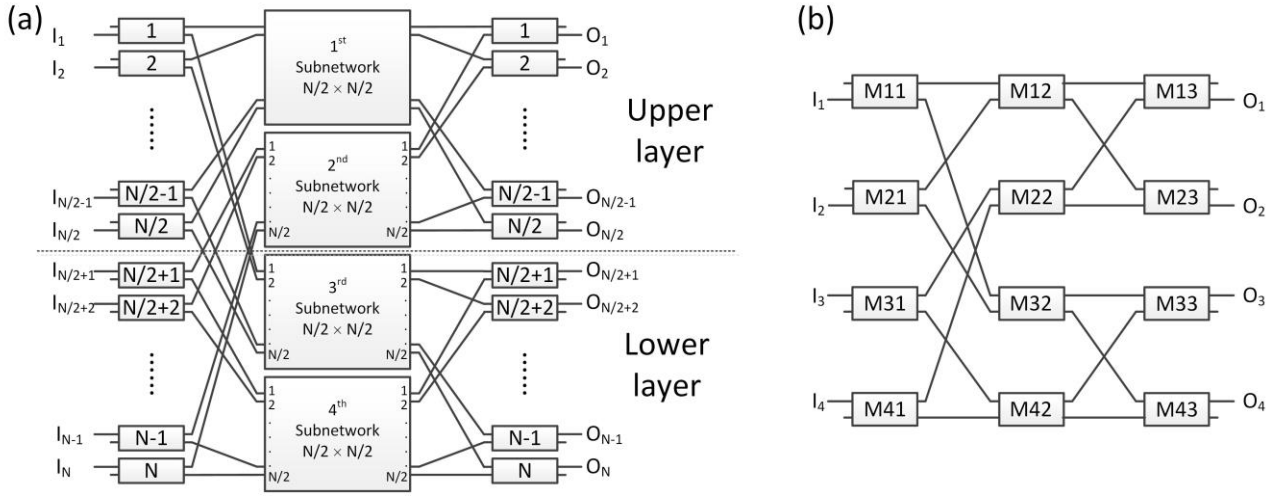

Fig. 1. (a) Architecture of the N×N DLN optical switch fabric. (b) Schematic of 4×4 DLN optical switch.

2.2. Chip design and fabrication

The proposed 4×4 DLN optical switch is designed for transverse electric (TE) polarization. The waveguides are based on silicon ridge waveguides with the width and height of 500 nm and 220 nm, respectively. The height of the slab layer is 60 nm. The switch elements are based on 2×2 symmetrical MZIs for broadband operation. The MZI element consists of two 2×2 multimode interferometers (MMIs) and two active waveguide arms, as illustrated in Fig. 2(a). The width and length of 2×2 MMI couplers are 5 μm and 29.5 μm, respectively. The input and output waveguides are linearly tapered from 0.5 μm to 1.2 μm in a length of 10 μm to reduce the excess loss. The measured insertion loss of the 2×2 MMIs is ~0.22 dB [17]. To realize TO and EO switching in the same device, the waveguide arms are integrated with both TiN micro-heaters and p-i-n diodes as shown in the inset of Fig. 2(a). The length of the active arms is 400 μm. The width of the TiN heater is 2 μm, which is the minimum feature size according to the foundry design rule. In order to suppress the thermal crosstalk and lower the TO power consumption, two air trenches are etched beside the waveguide arms. There are 8 waveguide crossings in the switch chip, which are based on 90°-crossed 1×1 MMIs. The crossings have a low insertion loss of 0.05 dB around the 1550 nm

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wavelength [17].

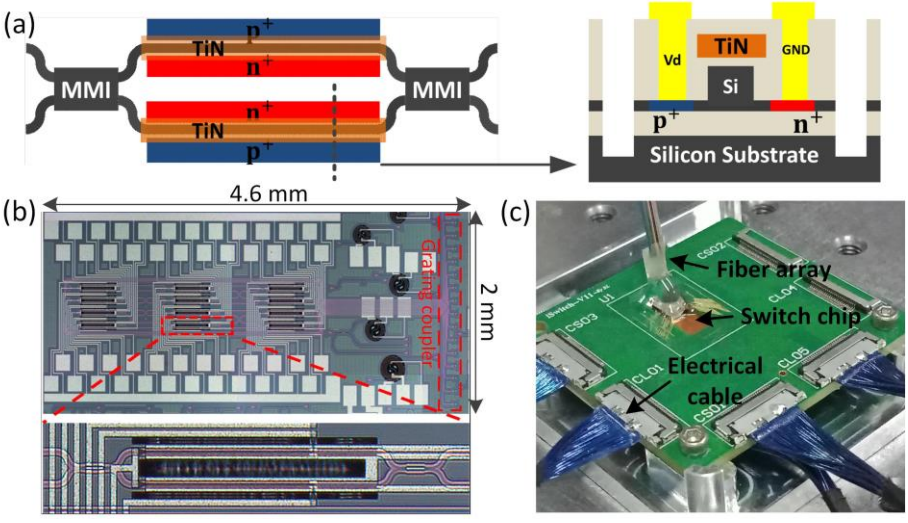

Fig. 2. (a) Schematic structure of the 2×2 MZI switch element. The inset shows the cross-section of the waveguide arm. (b) Microscope image of the fabricated silicon 4×4 DLN optical switch chip. (c) Photo of the packaged chip.

The chip was fabricated on an SOI wafer with a top silicon layer thickness of 220 nm and a buried oxide layer thickness of 2 μm. The fabrication was done using CMOS-compatible processes in AMF, Singapore. All the components are custom designed. Fig. 2(b) shows the microscope image of the fabricated 4×4 DLN switch. Grating couplers are used for light coupling in and out of the chip. All the grating couplers are placed in an array with a pitch of 127 μm at the right edge of the chip. The distance between the grating couplers and the rightmost electrodes is ~1 mm, which is reserved for coupling with a commercial fiber array. The chip footprint is 4.6 mm × 2 mm, including all the electrical pads and the input/output gratings. The footprint of a single MZI element is 70 μm × 640 μm, and the pitch size between MZIs is 120 μm and 1040 μm in the longitudinal and lateral directions, respectively. The chip was home-packaged before measurement. The chip was attached to a copper submount for good heat sink. A printed circuit board (PCB) was used to set up electrical links with on-chip electrical pads. A 20-channel fiber array was coupled with the grating couplers and firmly attached to chip using refractive index-matched UV-curable adhesive. The coupling loss after optical packaging is ~5.5 dB/facet, with a 1-dB bandwidth of 35 nm. Fig. 2(c) shows the picture of the chip after electrical and optical package. The whole packaged chip was held in a box during the test. A multi-channel voltage source was used to tune the switching states.

3. Experimental results

3.1. TO switching performance

We first adjusted the TO tuners to change the switching states. The chip was implemented as a 4×4 TO switch. As there is no multipath interference in the chip, it is very convenient to adjust the switching states of the 2×2 MZIs in the routing path by maximizing the power from the designated output port, while minimizing the output power of the rest ports. Therefore, all the elements can be tuned to the cross and bar states one by one. Table 1 lists the power consumption of all the switch elements when they are thermally switched to the cross and bar states, respectively. For each 2×2 MZI, TO tuners in the two arms are turned on individually for these two states, in which the shifted phases are both less than π. The summation of the shifted phases is π. Therefore, all the switch elements have a similar power efficiency of around 34 mW/π. The TO power efficiency can be further improved by etching undercut structures beneath the waveguides or by densely placing the routing waveguide underneath the TiN heater with geometrical optimization [26, 27]. The switching power for the cross state is lower than that for the bar state, which means the initial phase difference induced by fabrication is less than π/2.

Table 1 Power consumption of the switch elements for TO switching (unit: mW).

SE	Cross	Bar	SE	Cross	Bar
M11	14.74	19.23	**M12**	10.89	22.77
M13	13.94	19.64	**M21**	5.55	28.0
M22	5.40	29.75	**M23**	2.23	31.72
M31	1.60	31.42	**M32**	3.90	29.96
M33	4.79	28.08	**M41**	8.64	24.20
M42	10.02	23.90	**M43**	15.46	16.99

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We measured the transmission spectra of all the 24 switching states in the wavelength range from 1520 nm to 1580 nm, as shown in Fig. 3(a). There are totally 96 transmission curves and 288 crosstalk curves in the plot, which are all normalized with a test waveguide. In the measured 60 nm wavelength range, the overall crosstalk is lower than -20 dB. Fig. 3(b) shows the extracted on-chip insertion loss of all the 24 switching states at the 1550 nm wavelength. The average on-chip insertion loss is 1.74 dB, with a loss variation of ±0.59 dB. The loss variation is mainly contributed by the difference in the coupling loss for different ports, the waveguide crossing number in the routing paths, and the length of the connection waveguides. Fig. 3(c) shows the accumulated crosstalk at the four output ports of all the 24 states at the 1550 nm wavelength. The accumulated crosstalk for any routing path is defined as the summarized crosstalk contributed by all the noise paths. For a 4×4 optical switch, there are 3 noise paths for each routing path. We can see that the crosstalk values of 8 states are higher than the others. It is because two routing paths share the same switch element of the middle stage in these states, and the crosstalk is contributed by the first-order noise of the switch in the middle stage. In these states, the applied switching voltages of the middle stage switches are carefully tuned to get balanced crosstalk from both of the two routing paths. The worst crosstalk is -29.1 dB, which indicates the relatively low crosstalk of the 2×2 MZI switch. The rest routing paths suffer from the second-order noise of the switch elements. The crosstalk is lower than -45 dB, which is mainly limited by the leaked noise from the waveguide crossings. We also measured the temporal response for TO switching, which has the rise and fall time of 56 μs and 16 μs, respectively.

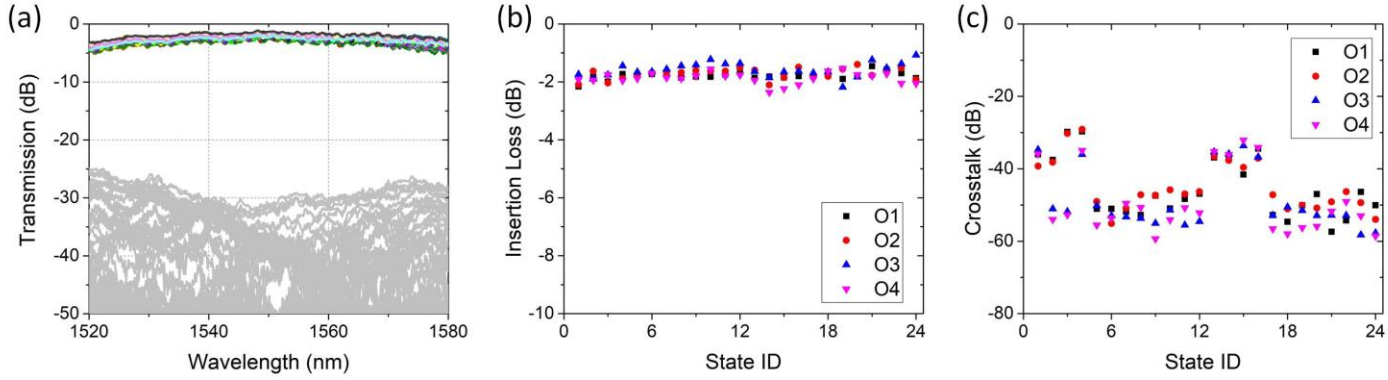

Fig. 3. (a) Measured transmission spectra of all the 24 switching states when the 4×4 DLN switch is thermally tuned. (b) Extracted on-chip insertion loss of each routing path at the 1550 nm wavelength. (c) Accumulated crosstalk to the four output ports from all noise paths at the 1550 nm wavelength.

3.2. EO switching performance

Next, we measured the switching performance when the EO tuners were used to change the states of the switch. To be mentioned, all the TO tuners are turned off during the EO switching. We also applied voltages to separate p-i-n diodes in the MZI arms for the cross and bar states. The tuning method is the same as the previous one. Table 2 lists the EO power consumption of all the switch elements at the cross and bar states, respectively. The power consumption for EO switching is around 7 mW/π.

Table 2 Power consumption of the switch elements for EO switching (unit: mW).

SE	Cross	Bar	SE	Cross	Bar
M11	2.28	4.44	**M12**	2.03	3.35
M13	3.28	4.01	**M21**	1.75	5.94
M22	0.92	6.70	**M23**	0.92	5.89
M31	0.72	7.53	**M32**	0.72	5.42
M33	1.43	5.58	**M41**	1.54	5.39
M42	2.31	5.75	**M43**	3.15	2.88

Fig. 4(a) shows the measured the transmission spectra of all the 24 switching states upon EO tuning. Due to the free carrier absorption effect, the insertion loss is higher compared with the TO switching. It also degrades the crosstalk of the 2×2 MZI switches, due to the imbalanced transmission loss of the waveguide arms. In the 60 nm wavelength range, the worst crosstalk is -18 dB. We also extract the on-chip insertion loss of all the 24 switching states at the 1550 nm wavelength, as depicted in Fig. 3(b). The average on-chip insertion loss is increased to 3.79 dB, with a loss variation of ±1.32 dB. The loss degradation is less than our previous work [17, 28], because smaller phase shifts (< π) are applied to the MZIs for the bar and cross states. Fig. 4(c) shows the accumulated crosstalk at the four output ports extracted from Fig. 4(a). The crosstalk performance can be also classified into two groups depending on whether the routing paths share the same middle stage elements or not. The worst crosstalk is -19.4 dB. We also notice that State #13 has a better crosstalk value of ~-30 dB even though paths I_1-O_4 and I_2-O_3 share M32 and paths I_3-O_4 and I_4-O_1 share M22. Both M32 and M22 are at the cross state. As the tuned phases in M32 and M22 is very small (see Table 2), the degradation due to EO shifting is negligible. Therefore,

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these two switches still have low crosstalk of ~-30 dB. The variation in insertion loss and crosstalk is mainly caused by the randomly tuned phases for the cross and bar states due to the fabrication errors. It can be further improved by initially adjusting the phase difference of the MZI arms to $\pi/2$ by the lossless thermal tuning. In that case, the insertion loss and crosstalk of different routing paths can be much more balanced. The rise and fall time of EO switching is 3.2/2.5 ns [17].

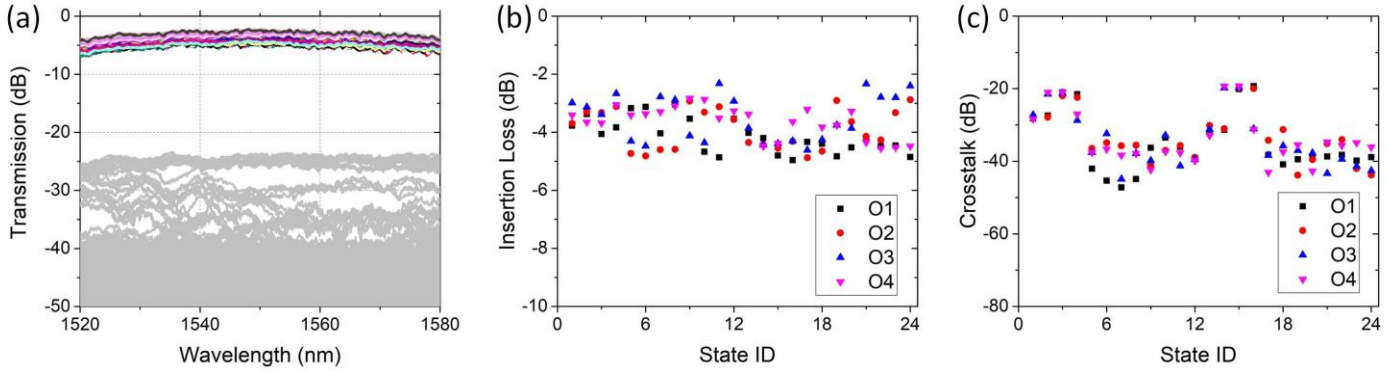

Fig. 4. (a) Measured transmission spectra of all the 24 switching states when the 4×4 DLN switch is EO tuned. (b) Extracted on-chip insertion loss of each routing path at the 1550 nm wavelength. (c) Accumulated crosstalk to the four output ports from all noise paths at the 1550 nm wavelength.

3.3. QPSK data transmission

Finally, we present the quadrature phase-shift keying (QPSK) optical signal transmission experiment to verify the routing performance of the fabricated silicon 4×4 DLN switch. Fig. 5 shows the experimental setup. A continuous wave (CW) light at the 1550 nm wavelength is generated by a tunable laser source (TLS). The light is modulated by a commercial $LiNbO_3$ in-phase/quadrature (IQ) modulator to generate the optical QPSK data stream. The IQ modulator is driven by two 32 Gb/s 2^{31}-1 pseudo-random binary sequence (PRBS) signals from two pulse-pattern generators (PPGs). Therefore, the bit rate of the optical signal is 64 Gb/s. The optical signal is amplified by an erbium-doped fiber amplifier (EDFA) and set the TE polarization before coupling to the switch chip. A variable optical attenuator (VOA) is used to adjust the output power to -10 dBm before analyzed by an optical modulation analyzer (Keysight, N4392A). We measured the constellation diagrams and the error vector magnitudes (EVMs) of the transmitted QPSK signals.

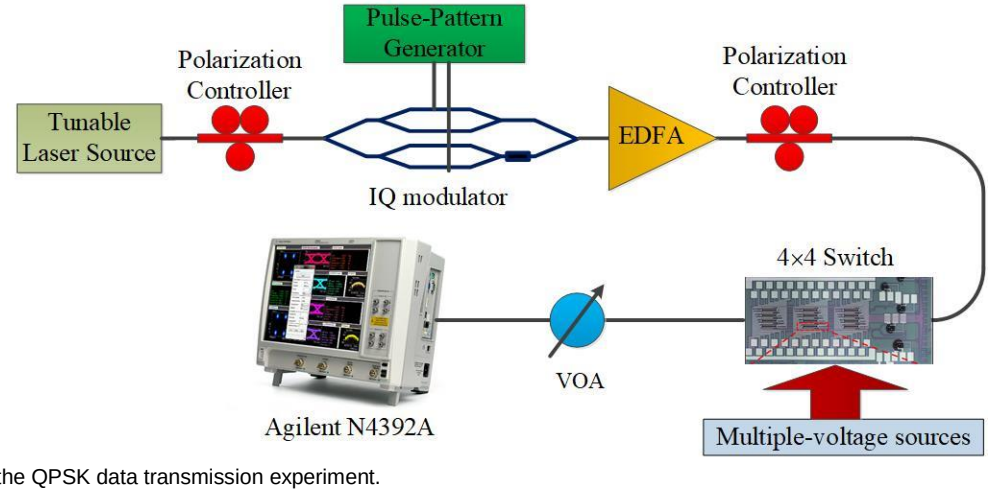

Fig. 5. System setup for the QPSK data transmission experiment.

Fig. 6(a) illustrates the constellation diagram of the system back-to-back transmission. Figs 9(b) and 9(c) show the constellation diagrams for four representative operation states when the chip is TO and EO switched, respectively. There is no observable signal degradation from the constellation diagrams. The measured EVMs of all the transmission are in the range from 11% to 12%, indicating the good signal integrity after passing through the chip. These results demonstrate that our 4 × 4 DLN switch can switch a 64 Gb/s QPSK signal.

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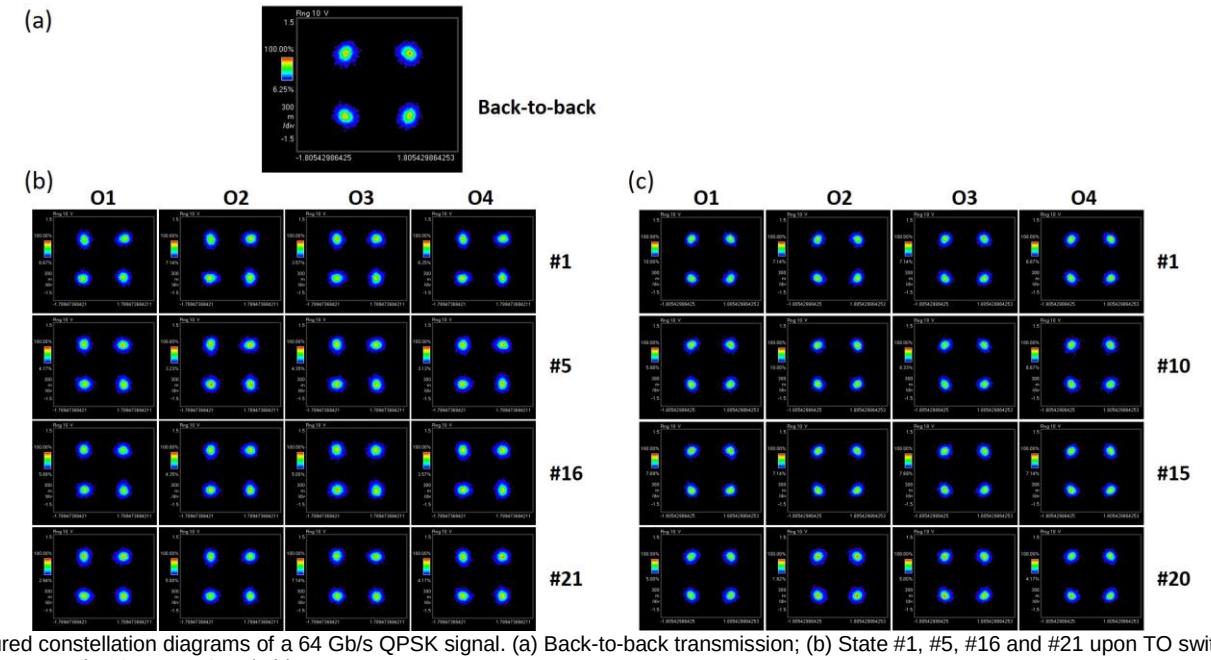

Fig. 6. Measured constellation diagrams of a 64 Gb/s QPSK signal. (a) Back-to-back transmission; (b) State #1, #5, #16 and #21 upon TO switching; (c) State #1, #10, #15 and #20 upon EO switching.

4. Comaprison and conclusions

We compare the switching performances of our switch chip with several previously reported silicon 4×4 optical switches, as illustrated in Table 3. For TO switching, our device shows the lowest insertion loss, and relatively low crosstalk and a broad operation bandwidth. For EO switching, as our 4×4 switch only turns on EO phase tuners, the insertion loss and crosstalk are inferior to that in [16]. However, the EO switching performances are still better than other silicon EO switches.

Table 3 Performance comparison with the reported silicon 4×4 optical switches.

Year	Technol.	Insertion loss (dB)	Crosstalk (dB)	Footprint (mm^2)	Power (mW)	Bandwidth (nm)
2013 [19]	EO MZI	9~11	-12	-	4.46~35.92	80
2015 [16]	TO+EO MZI	1.5~3	-25	5×3	12+24	15
2015 [20]	TO+EO DR-MZI	4~5.8	-18.4	3.4×1.6	22.37+1.38	0.28
2015 [28]	TO+EO MZI	5.8~7.7	-12	3.4×14	33.7+14.3	50
2016 [29]	TO MZI	4.8±0.5	-30	-	193	2.9
2018 [13]	EO MRR	6.9	-13.6	3.47×2.43	-	0.37
2019 [30]	TO MRR	1.8~20.4	-50	1.5×2.4	80	0.19
This work	TO MZI	1.74±0.6	-29.1	4.6×2	201	60
	EO MZI	3.79±1.3	-19.4		42	60

In conclusions, we have demonstrated a 4×4 strictly non-blocking silicon optical switch fabric based on the DLN architecture. Both the waveguide arms of the MZI elements are integrated with TO tuners and EO tuners. Therefore, we realized both TO and EO switching with the fabricated chip. The TO and EO switching power consumption is 34 mW/π and 7 mW/π for the MZI switch elements, respectively. We measured the transmission spectra of all the 24 states. The on-chip insertion loss is 1.74 ± 0.59 dB for TO switching and 3.79 dB ± 1.32 dB for EO switching at the 1550 nm wavelength. The worst crosstalk is -29.1 dB and -19.4 dB for TO and EO tuning, respectively. High-speed QPSK data transmission experiments reveal the good routing capability of the chip. These results verify the balanced performance in loss and crosstalk of the DLN architecture. Our silicon 4×4 DLN switch is a promising candidate for both optical circuit switching and optical packet switching for future all-optical switching networks in versatile application scenarios.

Acknowledgments

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