Silicon-based tunable optical delay lines and switches for next generation optical telecommunications

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ABSTRACT

We report our recent progress on reconfigurable optical true time delay lines (RTTDL) and optical switches. The RTTDL is composed of 8 stages of MZIs connected by 7 waveguide pairs with an incremental length difference. Variable optical attenuators are inserted in the delay waveguides to suppress crosstalk caused by the residual signals from noise paths. Transmission of a 25 Gbps PRBS signal confirms the signal fidelity after a maximum of 1.27 ns delay. The optical switch is based on a Benes architecture with Mach-Zehnder interferometers (MZI) as the switching elements. Both *p-i-n* diodes and silicon resistive micro-heaters are integrated in the MZI arms for electrical tuning and phase correction, respectively. The measured on-chip insertion loss of the 4×4 switch is < 8 dB. Transmission of a 50 Gb/s quadrature phase shift keying (QPSK) optical signal verifies its switching functionality.

Keywords: silicon photonics, optical signal processing, optical delay lines, optical switches

1. INTRODUCTION

The development of next generation optical telecommunications requires higher date rates to increase transmission capacity and all optical signal processing to reduce system complexity and power consumption [1]. All optical buffers and switches are the two key enabling functions in node signal processing. Optical buffers can be used for packet synchronization and contention management [2-4], while optical switches provides agile signal routing from multiple sources to multiple destinations with transparent transmission [5].

Optical signals cannot be directly stored as in electrical buffers, and therefore, optical buffers are always realized by optical delay lines in which signal buffering is achieved by time delay rather than photon storage. The time delay is equal to the optical path length divided by the optical group velocity: $\tau = L/v_g$. One way to get an optical delay is to use slow light devices where the required delay is obtained by slowing down light velocity in a waveguide or photonic structure. Optical delay lines based on microring resonators [6, 7], photonic crystals [8], gratings [9], and stimulated Brillouin scattering [10, 11] have been demonstrated. However, these slow light devices have a relatively narrow optical bandwidth and the delay capacity is limited by the delay-bandwidth product. Optical loss is also an issue for resonant slow light structures. Another method to get an optical delay is to physically increase the optical path length. A 27 meter long ultra-low-loss true time optical delay line has been implemented on a silicon chip recently [12]. Reconfigurable true time delay line (RTTDL) can be realized by cascading switches and optical delay lines of varied lengths [13]. As the number of optical paths is limited, delay can only be tuned discretely. RTTDLs integrated on various waveguide platforms have been successfully demonstrated, such as 4-bit RTTDL using polymer optical switches and waveguide delay lines [14], silica-based RTTDL fabricated by the planar lightwave circuit technique [15], 4-bit RTTDL using thermo-optic switches based on Si_3N_4 planar platform [16]. Silicon RTTDLs have also been proposed to leverage the high integration capability of silicon photonics [17, 18].

Large scale optical switches can be implemented by microelectromechanical systems (MEMS) and silica planar lightwave circuits (PLC) [5]. However, these devices have large footprint, high tuning power consumption, and low operation speed. Silicon based optical switches can have much compact device sizes, and meanwhile, free carrier

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plasma dispersion effect (FCD) can provide GHz switching speed. The switching elements can be microring resonators (MRR), Mach-Zehnder interferometers (MZI), or MZI-coupled MRRs [19-23] . Both MRR and MZI switches have their advantages: the MRR switch has a small footprint and low tuning power, while the MZI switch has a broad optical bandwidth and better tolerance to environment temperature variation.

Here we report our recent progress on the design and realization of silicon RTTDLs and switches [24-26]. The 7-bit RTTDL can provide 1.27 ns delay with a 10 ps resolution. The 4×4 MZI switch can provide 24 states of non-blocking switching with integrated *p-i-n* diodes and resistive micro-heaters. Optical signal transmission experiments are performed on both devices.

2. OPTICAL DELAY LINE

Figure 1(a) shows the schematic structure of an N-bit RTTDL consisting of N+1 stages of 2×2 MZI switches and N stages of waveguide pairs. Optical delay is varied by selecting different optical routing paths by the MZI switches. The delay difference of the waveguide pair in the N^{th} stage is $2^{N-1}\Delta t$ with Δt being the delay step. The tuning range of the N-bit RTTDL is from 0 to $(2^N-1)\Delta t$ relative to the reference path. In our design, we choose N = 7 and Δt = 10 ps so that the maximum delay is 1.27 ns. Figure 1(b) shows the 2×2 MZI switch composed of multimode interference (MMI) couplers. A *p-i-n* diode is embed in one arm to enable fast electrical tuning of the waveguide refractive index. The inset shows the cross-sectional schematic of the *p-i-n* diode. The refractive index change is based on the FCD effect. However, the free carrier absorption loss (FCA) is always accompanied, which reduces the transmission power upon tuning. As a result, the power imbalance in the MZI arms lowers the extinction ratio of MZI at the bar state, leading to a higher crosstalk than the cross state. To solve this issue, we insert variable optical attenuators (VOA) in each waveguide pair as depicted in Fig. 1(a) to attenuate the undesired residual signal [25]. The VOA is structurally similar to the phase shifter in Fig. 1(b), except that it takes advantage of the FCA to attenuate the optical wave when a positive voltage is applied.

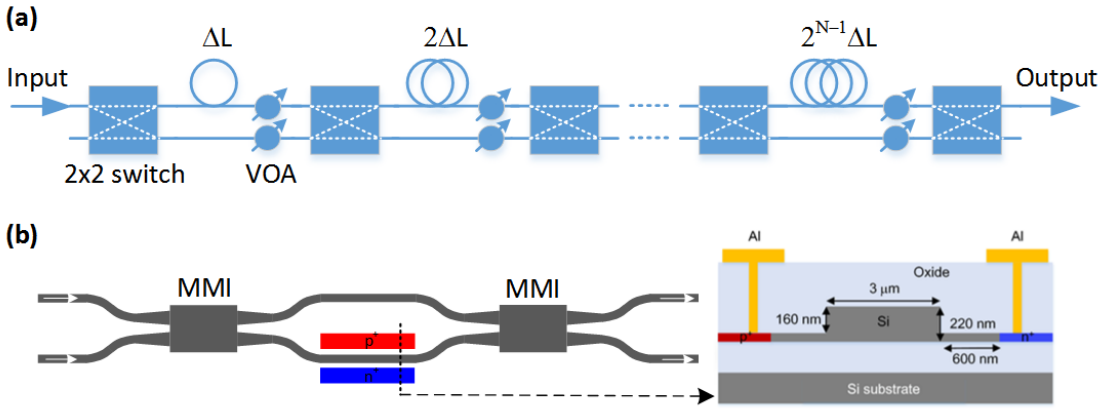

Figure 1. (a) Schematic illustration of an N-bit RTTDL. (b) 2×2 MZI switch with one arm actively modulated. Inset shows the *p-i-n* diode integrated on the MZI arm for optical phase tuning.

The device was fabricated using the CMOS fabrication processes from IME Singapore on a 220 nm silicon-on-insulator (SOI) wafer. 248-nm deep ultra-violet (DUV) photolithography was used to pattern the device and followed by plasma dry etch. p^+ and n^+ doping were performed with boron and phosphorus ion implantations with a doping concentration of ~10^{20} cm^{-3}. Silicon dioxide was upper clad on top of silicon waveguides using plasma-enhanced chemical vapor deposition (PECVD). The contact holes were finally etched followed by Aluminum (Al) layer patterning to form electrical connection. Figures 2(a) shows the mask layout of the device. The device area is 7.4 mm × 1.6 mm = 11.84 mm^2. It should be noted that multiple U-bend waveguides are used for the long delay waveguides to reduce the device footprint. Light is coupled into and out of the device through on-chip grating couplers using an 8-deg polished optical fiber array with a pitch of 127 μm. Figure 2(b) shows the fabricated chip

incorporating two 7-bit and two 5-bit RTTDLs together with other test devices. As multiple supply voltages are needed to drive the chip, we wire-bonded the chip to a printed circuit board (PCB) using 25-μm-diameter gold wires. Figures 2(c) and 2(d) show the packaged chip on a PCB.

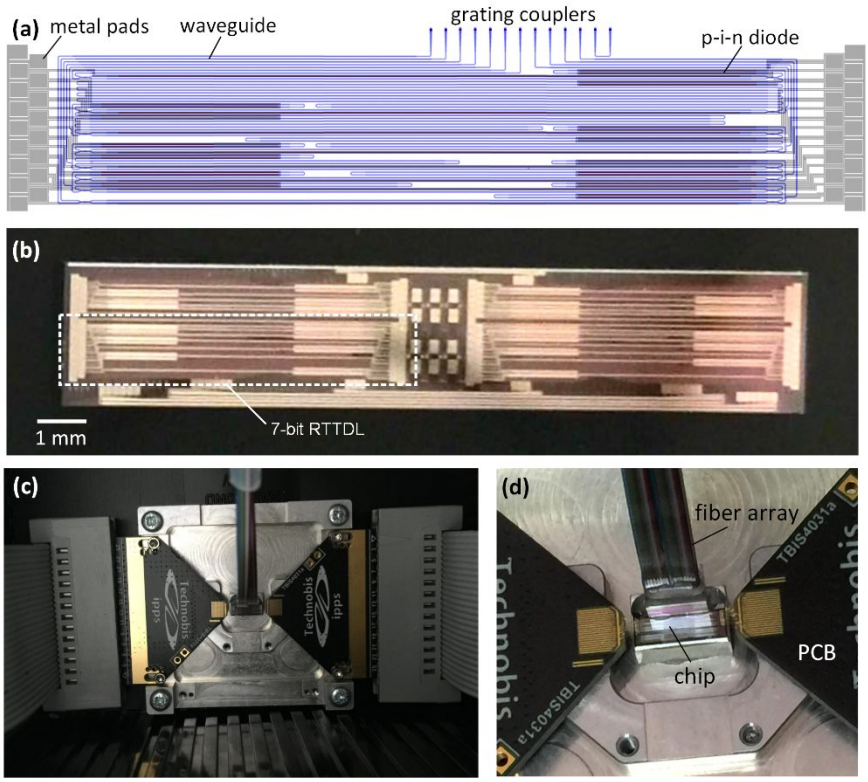

Figure 2. (a) Mask layout of the 7-bit RTTDL. (b) Photograph of the fabricated chip. (c) Chip packaged with a PCB and a fiber array. (d) Zoom-in view of the packaged chip.

We characterized the device by measuring the delays of optical pulses under various configurations. Laser light at 1550 nm was set to transverse electric (TE) polarization by a polarization controller, and modulated by a pulse pattern generator to generate a pulse train. The modulated signal was then amplified by an erbium-doped fiber amplifier (EDFA) followed by a bandpass filter before coupling into the device. The output optical signal was amplified by another EDFA to compensate for the device insertion loss. A 32 GHz bandwidth oscilloscope was used to record the output waveform.

Figure 3 shows the output waveforms with various delays. In each plot, both the reference (the shortest path) and delayed waveforms are shown. The relative delay increases from 10 ps to 640 ps when we switch on each stage (the long waveguide is selected) as shown by the first 7 plots. The maximum delay is 1.27 ns when all stages are switched as shown by the bottom plot. Hence, the RTTDL can provide 128 delays with a resolution of 10 ps. We also examine the quality of the delayed optical signal by measuring the eye diagrams. Figure 6 shows the eye diagrams of a 25 Gbps 2^{51} -1 pseudo-random binary sequences (PRBS) signal for the system back-to-back (BtB), the minimum, and the maximum delay transmissions. The eye diagram is degraded with the increasing delay primarily due to the increased insertion loss. It is worth noting that our device is broadband and the bandwidth is only limited by MMIs (other than grating couplers) which can cover 10's nm. For a 40 Gbps on-off keying (OOK) optical signal, our device can buffer 50.8 bits.

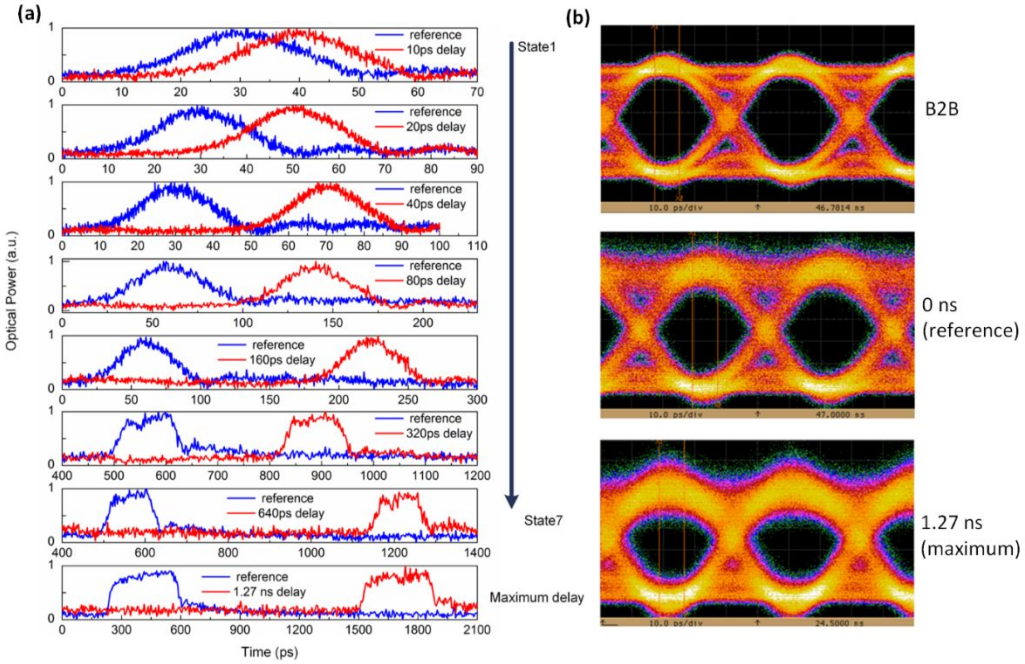

Figure 3. (a) Output optical waveforms showing 10 ps to 1.27 ns optical delays. (b) Comparison of eye diagrams for a 25 Gbps 2^{51} -1 PRBS signal.

3. OPTICAL SWITCH

Figure 4(a) shows the architecture of the 4×4 Benes switch fabric, consisting of three stages 2×2 switch elements. The Benes architecture has the minimum switching components and is non-blocking. Each routing path contains 3 switch elements, favoring balanced output power. There are totally 2^6=64 routing configurations for the 4×4 switch, among which some are redundant. Only 24 permutations are needed for non-blocking operation.

We use 2×2 MZI as the building block for the 4×4 switch. MZI arms are integrated with *p-i-n* diodes for fast electro-optic (EO) switching. When the *p-i-n* diode is turned on, free carriers are injected into the waveguide, the MZI is switched from the "cross" to the "bar" state, which we denoted as "0" and "1" states, respectively. The *p-i-n* diode can have a very fast switching speed up to GHz. In principle, one *p-i-n* diode is enough for switch operation. However, fabrication is never perfect and there is always phase errors in the long MZI arms. In order to correct phase errors, we also integrate resistive micro-heaters into the MZI arms. When current flows through the lightly doped waveguide, heat is generated and phase is changed due to thermo-optic (TO) effect. The EO and TO tuning arms are 356 and 89 μm long. As the fast switching is enabled by the *p-i-n* diode, there is an intrinsic limitation to the switching ER. For the cross-state without carrier injection, the two arms are perfectly balanced and light is transmitted to the cross-port with a high contrast between the two ports. For the bar-state, however, FCA is always present and reduces the optical power in the lower arm, making the two arms unbalanced. The incomplete interference introduces inter-symbol crosstalk to the signal.

The Benes architecture can also be scaled to a 16×16 switch fabric as shown in Fig. 4(c), where each routing path incorporates 7 stages of switch elements. One can see that more waveguide crossings are needed for the 16×16 switch, and thus it is important to design low-loss and low-crosstalk waveguide crossings.

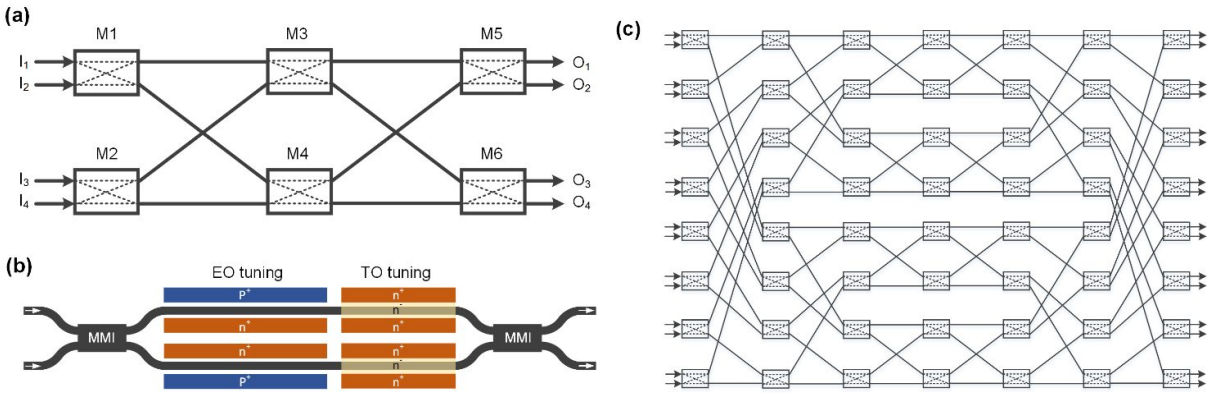

Figure 4. (a) 4×4 Benes switch architecture. (b) Schematic of the 2×2 MZI switch element. (c) 16×16 Benes switch architecture.

Figure 5(a) shows the mask layout of the 4×4 switch. The device area is 3.5 mm × 1.5 mm. The input and output waveguides are intentionally elongated to the left side to leave enough space for fiber array coupling with grating couplers. Figure 5(b) shows the mask layout of the 16×16 switch. It has a larger device area of 7 mm × 3.7 mm. As there are totally 56 switch elements to control, we put all the wire-bonding pads along the chip edges and grating couplers in the chip center. Figure 5(c) shows the packaged chip on a PCB with a fiber array attached using UV-adhesive.

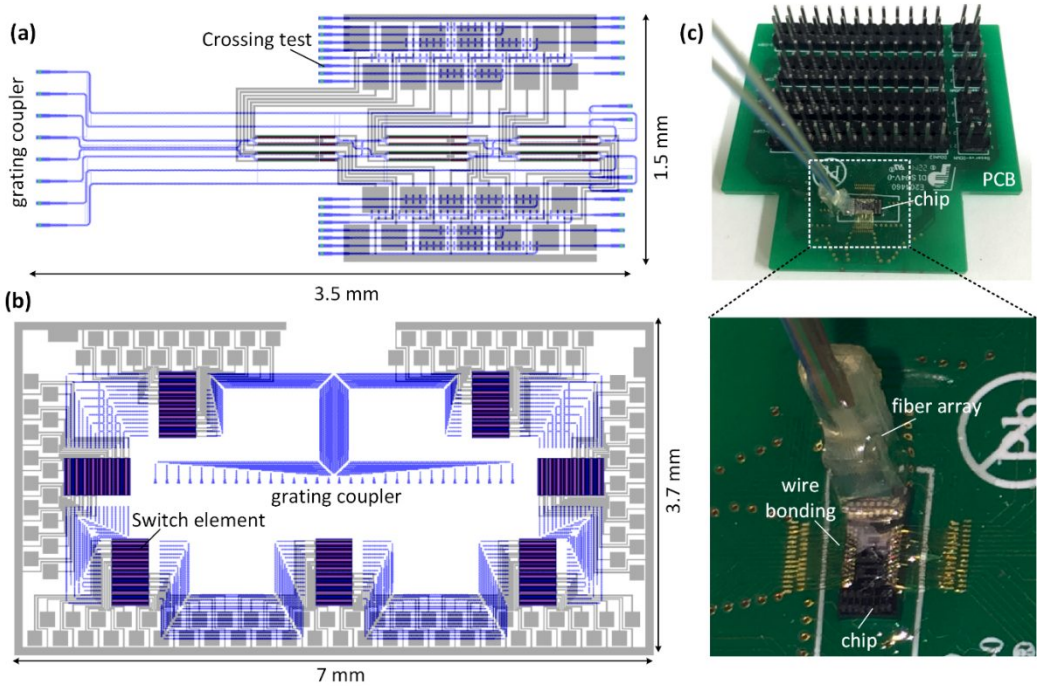

Figure 5. (a) Mask layout of the 4×4 switch. (b) Mask layout of the 16×16 switch. (c) 4×4 switch chip packaged with a PCB and a fiber array.

We first characterized the performance of waveguide crossings. 1×1 MMI is used at the crossing to reduce the insertion loss and crosstalk. Because of the self-imaging effect of MMI, input light is focused at the center of the crossing with greatly reduced divergence. Figure 6(a) shows the test pattern for the waveguide crossings. The width

and length of the MMIs are 1.7 and 8.14 μm, respectively. The measured spectra of 50, 100 and 150 crossings together with a reference waveguide are shown in Fig. 6(b), and the extracted insertion loss per crossing is shown in Fig. 6(c). The insertion loss is around 0.03 dB and the crosstalk is better than -25 dB around 1570 nm. We then characterized the performance of 2×2 MMIs which are critical components in MZI switches. The test pattern consists of 7 stages of MMIs (Fig. 6(d)). From the measured transmission spectrum of Fig. 6(e), we can derive the splitting loss per 2×2 MMI is around 3 dB around 1570 nm as shown in Fig. 6(f), indicating the MMI has a near 50:50 splitting ratio.

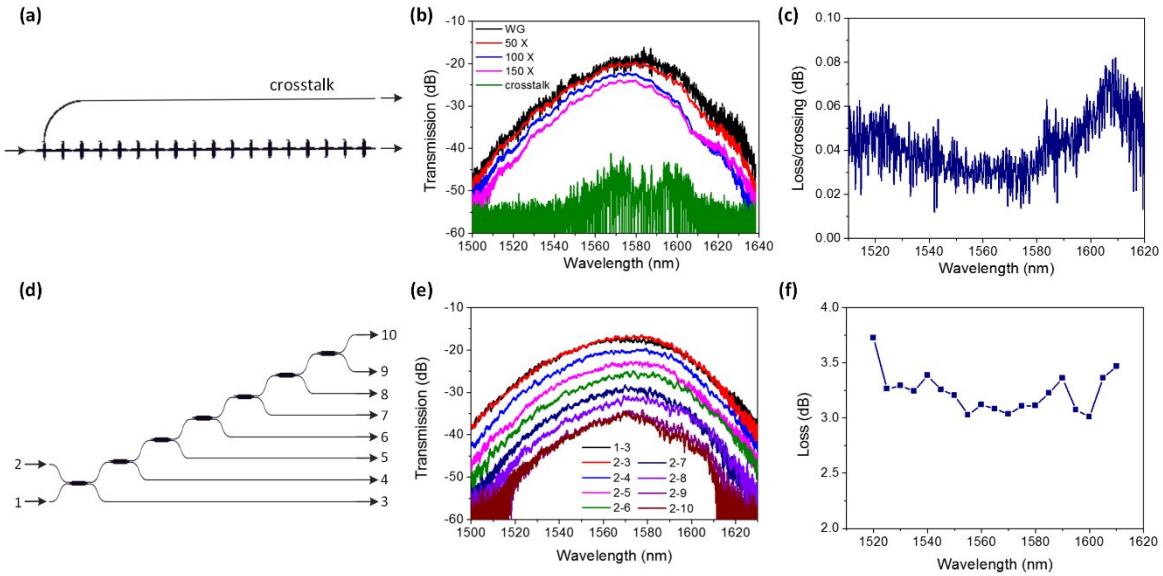

Figure 6. (a) MMI crossing test structure. (b) Measured transmission spectra of the MMI crossings. (c) Extracted insertion loss per MMI crossing. (d) 2×2 MMI test structure. (e) Measured transmission spectra of the 2×2 MMI. (f) Extracted splitting loss of the 2×2 MMI.

Figure 7(a) shows the measured on-chip insertion loss of the 24 states of the 4×4 switch. The insertion loss has 2-3 dB variation because the MZI loss increases when it changes from the "cross" state to the "bar" state due to the FCA effect. Figure 7(b) shows the accumulated crosstalk of all 24 switching states. The accumulated crosstalk for a certain routing path is defined as the summation of crosstalk contributed by all noise paths. It can be seen that the accumulated crosstalk is better than -9.6 dB.

We also verified the switching functionality of the 4×4 switch by transmission of quadrature phase shift keying (QPSK) optical signals. The input was a 2^{31}-1 PRBS signal at a bit rate of 50 Gb/s. The transmitted signal was received and analyzed by an optical modulation analyzer (Agilent, N4392A). The error-vector-magnitude (EVM) was obtained from the measured constellation diagrams. Figure 7(c) shows the constellation diagrams of the "000000" and "111111" states, together with the system back-to-back (BtB) transmission. The BtB EVM is 12.9% and the EVM after device experiences slight deterioration but all less than 13.6%. It illustrates that our device is capable of switching 50 Gb/s QPSK optical signal with high signal integrity. Testing of the more complicated 16×16 switch is on-going.

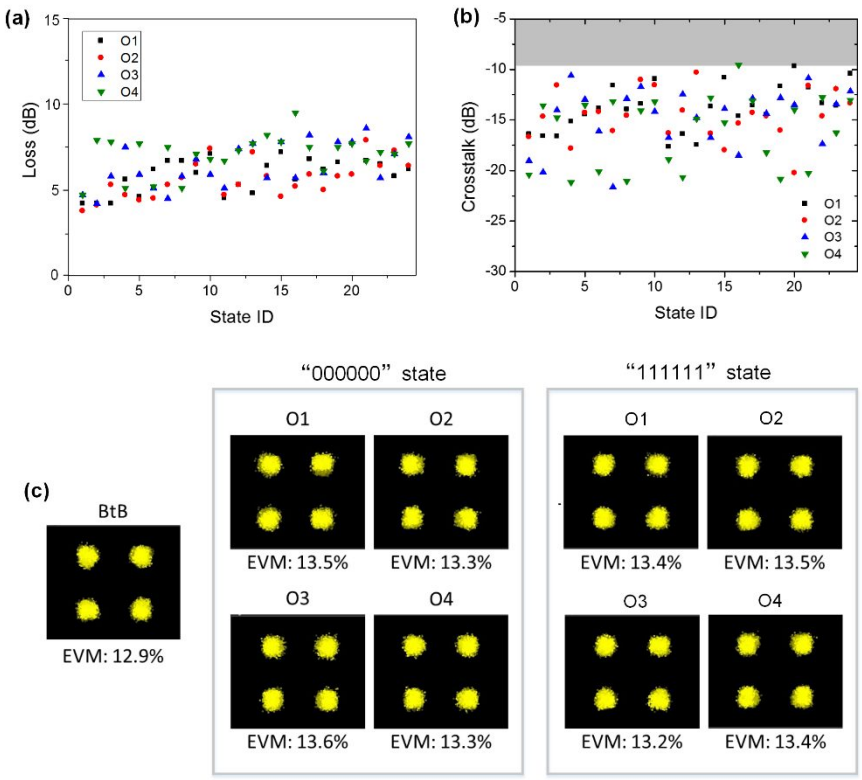

Figure 7. (a) On-chip insertion loss of each routing path for the 4×4 switch. (b) Accumulated crosstalk from all noise paths to the four output ports. (c) Measured QPSK constellation diagrams for the "000000" and "111111" states.

4. CONCLUSIONS

We have demonstrated reconfigurable optical true time delay lines and MZI-based optical switches on the silicon-on-insulator platform. The delay line consists of 7 stages of silicon waveguide pairs connected by 2×2 MZI switches. Variable optical attenuators are embed to suppress crosstalk caused by the finite extinction ratio of switches. The delay line can provide a maximum of 1.27 ns delay with a 10 ps resolution over a wide wavelength range. Eye diagram measurement of a 25 Gbps 2^{51}-1 PRBS signal reveals no significant degradation of signal quality. The 4×4 optical switch is composed of three stage of 2×2 MZI switches with integrated *p-i-n* diodes and silicon resistive micro-heaters, which can provide the full 24 states of non-blocking signal routing. Measurements show that the on-chip insertion loss of all 24 states is < 8 dB and accumulated crosstalk better than -9.6 dB at the 1550 nm optical communication band. The switching functionality was verified by the transmission of a 50 Gb/s QPSK optical signal.

5. ACKNOWLEDGEMENTS

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