Strictly Non-blocking 4×4 Silicon Electro-optic Switch Based on a Double Layer Network Architecture

Zhanzhi Guo, Liangjun Lu, Shuoyi Zhao, Linjie Zhou*, and Jianping Chen
State Key Laboratory of Advanced Optical Communication Systems and Networks
Department of Electronic Engineering, Shanghai Jiao Tong University, Shanghai 200240, China
*ljzhou@sjtu.edu.cn

***Abstract*—We report a 4×4 silicon switch based on a double layer network architecture by cascading three stages of electrically tunable Mach-Zehnder interferometers (MZIs). Preliminary experiment reveals that the switch has on-chip insertion loss less than 4 dB and crosstalk lower than -30 dB.**

Index terms — silicon photonics, optical switches, MZI, optical interconnection.

I. INTRODUCTION

With the growing demand for could computing and big data applications, the data centers have seen rapid development in recent years. Optical switching is necessary to establish the interconnect networks in data centers to provide high-speed, low-latency and low-power data exchange among high-performance servers [1]. Of the various technologies that can be used to build optical switches, silicon photonics is quite attractive as it has the merits of high integration, compatibility with microelectronic circuits, low cost and fast response [2, 3]. A variety of topological architectures have been used to build the N×N optical switches, such Benes, crossbar, switch-and-select etc. The basic criteria to choose the topology is non-blocking, low loss and low crosstalk. In our previous work, we have demonstrated 4×4 and 16×16 optical switches based on the Benes architecture [4-6]. The Benes switch requires the least number of switching elements (N/2·(N/2-1)) to realize non-blocking switching in a reconfigurable way. The crosstalk is relatively high due to the various interference paths existing in the Benes network. The crossbar is a strictly non-blocking switch architecture. It incorporates N^2 switching elements but the crosstalk is intrinsically lower than the Benes structure.

In this work, we demonstrate a 4×4 silicon switch fabric built using a double layer network (DLN). The DLN is strictly non-blocking [7]. It makes a good compromise between the Benes and crossbar architectures. Compared to other non-dilated architectures, DLN architecture has lower path loss and better crosstalk.

II. DEVICE STRUCTURE

Figure 1(a) shows the topological network architecture of the 4×4 DLN switch. It has 8 input and 8 output ports, but only 4 ports at each side are connected out for optical data switching. Each optical paths goes through three stages of switching elements, and thus the optical paths are balanced. It should be noted that the switching elements in the first and third stages are essentially 1×2 switches, and therefore, as long as the crosstalk of the switching elements in the second stage is low, the entire 4×4 switch chip can have low crosstalk.

The switching elements are based on Mach-Zehnder interferometers integrated with both TiN microheaters for thermo-optic (TO) tuning and p-i-n diodes for electro-optic (TO) tuning. The TO tuners are designed for phase error correction and the EO tuners for GHz speed switching. The design parameters are similar to our previous work [6].

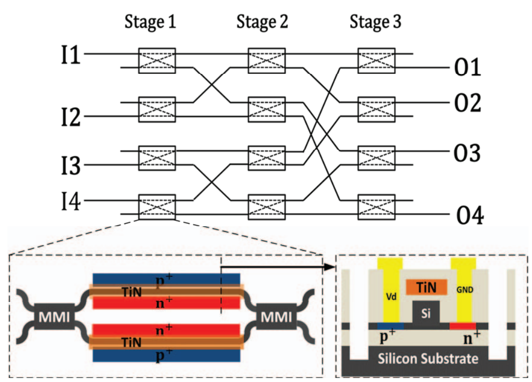

Fig. 1 Topological architecture of the 4×4 DLN switch. The inset shows the structure of the switching element based on a MZI.

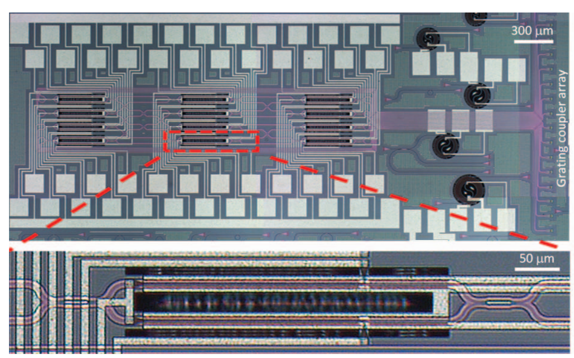

Fig. 2 Optical microscope image of the fabricated switch. The inset shows the zoom-in view of one MZI switching element.

Figure 2 shows the optical microscope image of the 4×4 switch fabric. The input and output waveguide ends are terminated with grating couplers with a pitch of 127 μm for

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coupling with a fiber array. The electrodes of TiN microheaters and p-i-n diodes are all connected to the metal pads. The chip was finally wire-bonded to a print circuit board for applying electrical signals.

III. Experimental Results

The 4×4 DLN switch has 24 states for all possible connections. We measured the transmission spectra for 2 typical states as shown in Figs. 3 and 4. The input polarization is TE and all spectra are normalized to a test waveguide. TO tuning was first performed to compensate the initial phase difference between MZI arms, so that all switching elements were in the “cross” state. The total TO power consumption is around 118.4 mW. The p-i-n diodes in some of the switching elements were then turned on to switch to the “bar” state to get the desired switching state. Here we only applied voltage to one p-i-n diode in each MZI switch to simplify the electrical switching. In principle, push-pull tuning of the p-i-n diodes can result in a lower crosstalk.

Figure 3 shows the measured spectra for switching state “1342”, which means the input-to-output connections are I1-O1, I2-O3, I3-O4, and I4-O2. There are 8 switching elements configured to the “bar” state. The average on-chip insertion loss is less than 4 dB around the 1550 nm wavelength. The crosstalk is less than -30 dB in the 60 nm wavelength range. The total EO power consumption is around 52 mW, resulting in 6.5 mW EO power consumption for each switching element on average.

Figure 4 shows another switching state “4213”. The connections become I1-O4, I2-O2, I3-O1, and I4-O3. Four switching elements are electrically turned on. The overall performance is similar to the previous case. The total EO power consumption is 20.3 mW.

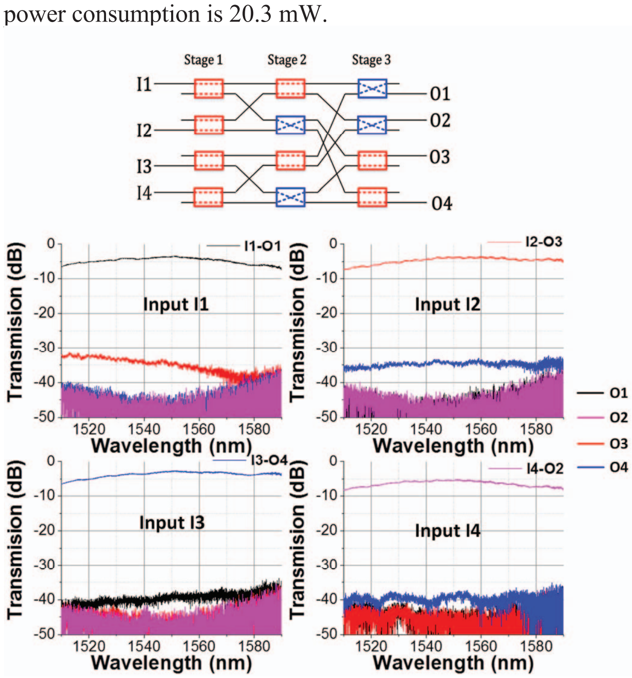

Fig. 3. Configuration for the switching state “1342” and the measured transmission spectra.

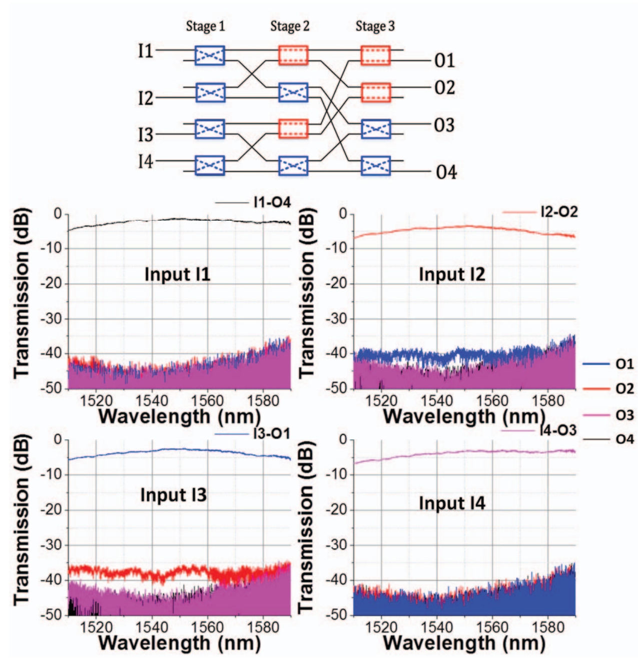

Fig. 3. Configuration for the switching state “4213” and the measured transmission spectra.

IV. Conclusion

We have demonstrated a strictly non-blocking 4×4 DLN silicon switch fabric with the MZI as the switching element. The MZI can be both thermally and electrically tuned by the integrated TiN microheater and the p-i-n diodes, respectively. The preliminary experimental results show that the switch has a low on-chip insertion loss of < 4 dB and low crosstalk of < -30 dB in a 60 nm wavelength range.

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