

Nanosecond-range Continuously Tunable Silicon Optical Delay Line Using Ultra-thin Silicon Waveguides

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Abstract: We report a continuously tunable optical delay line with the maximum delay > 1 ns by combining digital switchable delay line and microring slow light structures built on the 60-nm-thick silicon waveguide platform.

OCIS codes: (130.3120) Integrated optics devices; (230.5750) Resonators; (130.4815) Optical switching devices.

1. Introduction

Optical delay lines play a very important role in the areas of optical signal buffering, optical packet synchronization and photonic signal processing [1-2]. Generally, there are two approaches to generate delays for optical waves by either increasing the optical path length or by slowing down the light velocity in the waveguides. In our previous work, we have realized a silicon reconfigurable true time delay line (RTTDL) by using 8 stages of Mach-Zehnder interferometer (MZI) switches [3]. The maximum delay is 1.27 ns with the tuning resolution of 10 ps. On the other hand, we have also realized continuous delay tuning of 100 ps by using reflective side-coupled microring resonators [4]. These two types of delay line structures both have their pros and cons. The former one can provide large-range digitalized delays but the resolution is limited by the length difference of the delay waveguides; the latter one can realize continuous delay but the delay-bandwidth product is limited by the number of microrings. In this work, we present an optical delay line by combing these two structures to offer nanosecond continuous delay. To reduce the waveguide propagation loss, we use ultra-thin silicon waveguides to build our device [5].

2. Device structure

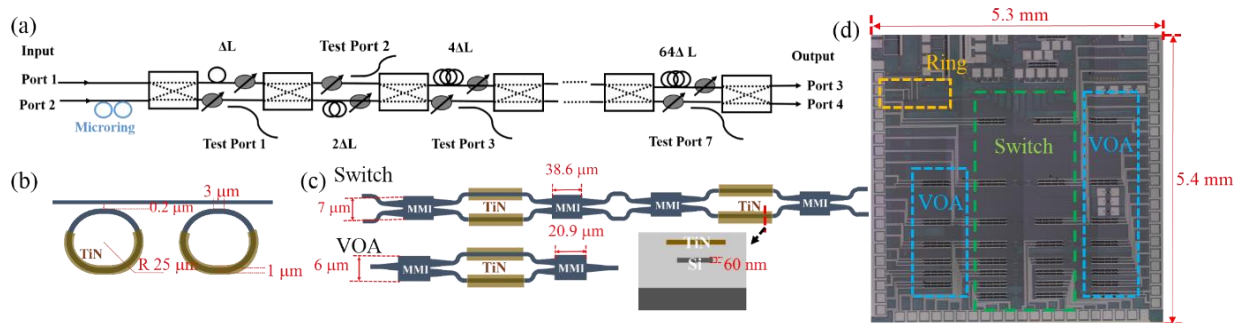


Fig. 1 (a) Architecture of the continuously tunable optical delay line structure. (b) Dual-microring slow-light delay line. (c) Structures of the 2×2 switch unit and VOA. Inset shows the cross-section of the thermo-optic phase shifter. (d) Optical microscope image of the fabricated device.

Figure 1(a) shows the schematic drawing of the continuously tunable silicon optical delay line. It is composed of two parts: a dual-ring slow light waveguide followed by a 7-bit switchable delay line (input from Port 2). The microrings provide continuous group delay tuning of t_{ring} upon thermally shifting the resonance wavelengths. The time delay given by the switchable delay line is variable by configuring the 8 switches to establish different optical routing paths. The lengths of the waveguides between switches are carefully designed so that the N^{th} stage provides an incremental delay of $2^{N-1}\Delta t$. Hence, for the 7-bit switchable delay line, the maximum delay is $127\Delta t$. In our design, we set $t_{\text{ring}} > \Delta t$, and therefore the entire delay line can provide a continuous delay tuning up to $t_{\text{ring}} + 127\Delta t$. Figure 1(b) shows the thermally tunable dual-ring delay line structure. The waveguide width is $1 \mu\text{m}$ and the height is 60 nm . Figure 1(c) shows the 2×2 switch and variable optical attenuator (VOA) structures. The switch is composed of two cascaded MZIs to ensure a high switching extinction ratio. The VOA is used to further eliminate the leakage optical power to the undesired optical paths so as to improve the signal-to-noise ratio of the delayed optical signals. TiN heaters are positioned above the silicon waveguides for thermal tuning of the microrings and MZIs. As the waveguides are long, we purposely widen the waveguide to $2.5 \mu\text{m}$ wide in the long straight sections

to ensure a low propagation loss. The wide waveguides are connected to thin waveguides through 60- μm -long tapers. Figure 1(d) shows the microscope image of our fabricated chip. Grating couplers are used to couple light in and out of the device. All the electrical pads are wire-bonded to a printed circuit board (PCB).

3. Experimental Results

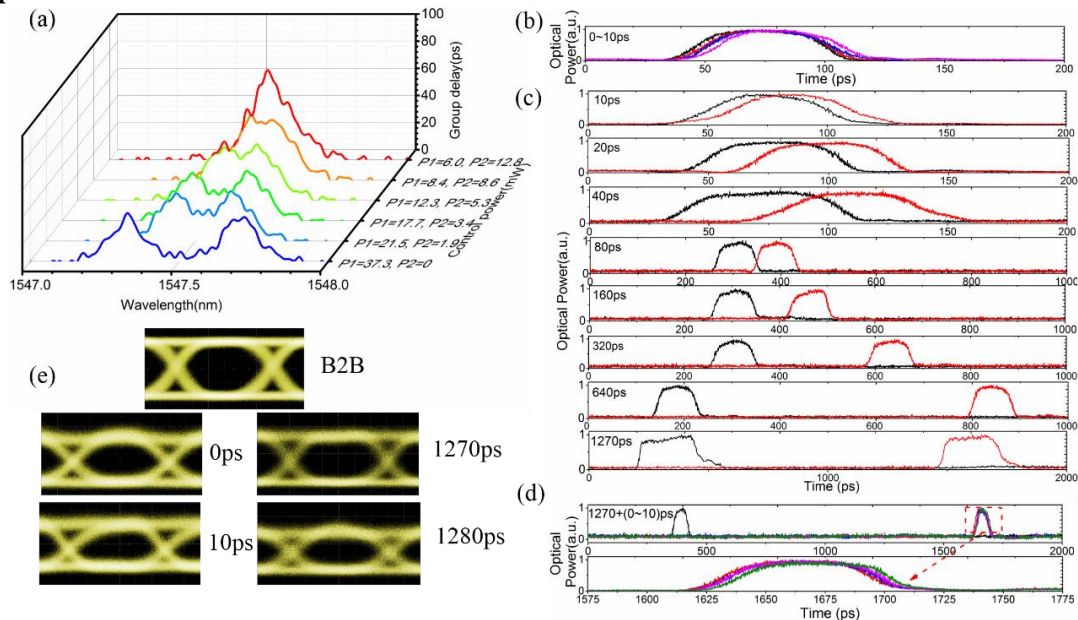


Fig. 2 (a) Evolution of the microring delay line group delay spectrum. (b) Optical pulse waveforms after passing through the microring delay line. (c) Optical pulse waveforms after passing through the switchable delay line. Black curves: reference pulses; red curves: delayed pulses. (d) Optical pulse waveforms after passing through the entire delay line. (e) Eye diagrams of a 30 Gbps $2^7 - 1$ PRBS signal before and after various delays.

Figure 2(a) shows the group delay spectra of the microring delay line under various tuning power. The push-pull differential tuning method is used [4]. The input is from Port 2 and the output is from Test Port 1 with the first switch configured at the bar state. When the two rings resonate at the same red-shifted wavelength (~ 1547.5 nm), the group delay reaches the maximum of 66 ps. Then one ring is blue-shifted by decreasing the applied power while the other ring is red-shifted by increasing the power. As a result, the group delay is continuously decreased down to 0 ps when the two group delay peaks are fully separated. Figure 2(b) shows the optical pulses with delay continuously tuned within 10 ps. Figure 2(c) shows the optical pulses after various digital delays (resolution $\Delta t = 10$ ps) given by the switchable delay line. The relative delay increases from 10 ps to 640 ps as shown by the first 7 plots when only one delay stage is turned on. When all stages are turned on, the delay reaches a maximum value of 1.27 ns. Figure 2(d) shows the optical pulses when the microring is tuned while the switchable delay is fixed at the maximum. It thus demonstrates that continuous delay tuning of 1.28 ns can be achieved. The on-chip insertion loss for the maximum delay is ~ 12.4 dB. We also measure the eye diagrams of a 30 Gbps $2^7 - 1$ pseudo-random binary sequences (PRBS) signal after passing through the delay line, as shown in Fig. 2(e). Clear and open eyes are observed after various delays.

4. Conclusions

We have demonstrated nanosecond continuous delay tuning in an optical delay line composed of microring and MZI switchable delay structures. The device is made using 60-nm-thick silicon strip waveguides to reduce the waveguide loss. The on-chip insertion loss is ~ 12.4 dB for the maximum 1.28 ns delay.

5. References

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