4 × 4 Nonblocking Silicon Thermo-Optic Switches Based on Multimode Interferometers

Liangjun Lu, Linjie Zhou, *Member, IEEE*, Shulin Li, Zuxiang Li, Xinwan Li, *Senior Member, IEEE*, and Jianping Chen

***Abstract*—We experimentally demonstrate a silicon 4 × 4 nonblocking thermo-optic (TO) switch using a generalized Mach–Zehnder interferometer constructed on multimode interferometers. All the 24 switching states for nonblocking switching are characterized. The device fabricated using CMOS technologies has a footprint of 2.8 × 0.65 mm^2. The measured average on-chip insertion loss is 9 ± 2 dB and the crosstalk for all switching states is better than –12 dB. The average TO switching power consumption is 109 mW. The switching functionality is verified by transmission of a 40-Gb/s quadrature phase-shift keying optical signal.**

***Index Terms*—Integrated optics, optical interconnections, optical switches.**

I. Introduction

INTEGRATED optical switches are practically demanded for both long-haul telecommunications and on-chip optical interconnects [1]–[3]. N × N optical switches are usually constructed by 1 × 2 or 2 × 2 switch elements, such as Mach-Zehnder interferometers (MZIs) [4]–[9] and microring resonators (MRRs) [10]–[12]. In comparison with MRRs, MZI-based switches have a broader optical bandwidth and better tolerance to environmental variations. In addition to directional couplers, one can also use multimode interferometers (MMIs) to form a MZI. The MMI is based on the self-image effect [13] and features compact size, broadband operation, and high tolerance to geometric deviations. It also supports multiple input and output ports. By connecting multi-port MMIs using an array of phase shifters, the so-called generalized Mach-Zehnder interferometer (GMZI) can be formed. The GMZI can function as a 1 × N or N × N switch [14]–[16]. Compared with switches formed by cascaded 2 × 2 MZIs, the GMZI switches have a simpler structure and a smaller footprint.

So far, most GMZI-based optical switches have been experimentally demonstrated on the III-V semiconductor platform [17]–[19] and the silica planar lightwave circuit (PLC) platform [20], [21]. The silicon platform, due to its high index contrast, low waveguide loss, and compatibility with complementary metal-oxide–semiconductor (CMOS) technology, has recently shown its potential for integrated optical switches [4]–[8]. To date, a few silicon switches based on GMZI have been reported. H. Zhou, *et al.*, proposed a silicon 1 × 4 GMZI switch [22]. W. Wang, *et al.*, demonstrated a 3 × 3 silicon thermo-optic (TO) switch with a single combined phase shifter [23]. Unfortunately, a single N × N GMZI switch only has N independent switching states [24] and hence cannot provide N × N non-blocking switching. This issue can be addressed by cascading a N×N GMZI with 2 × 2 MZIs. Such an architecture has balanced non-blocking light paths and no waveguide crossings [25], which eliminate crossing-induced loss and crosstalk, a merit more notable for large-scale optical switches. To the best of our knowledge, there has been no experimental demonstrations of N × N non-blocking GMZI switches yet.

In this paper, we report the first experimental realization of a silicon 4 × 4 non-blocking optical switch based on GMZI. The device footprint is 2.8 × 0.65 mm^2. The measured crosstalk for all switching states is better than −12 dB and the on-chip insertion loss is within 9 ± 2 dB at the optical telecommunication band. The switching functionality is verified by transmission of a 40 Gb/s quadrature phase-shift keying (QPSK) optical signal. The rest of the paper is organized as follows. Section II gives the detail of the switch architecture. Section III presents an overview of the device structure and the fabrication process. Next, we present the experimental measurement and characterization of the device in Section IV. In Section V, we discuss how the power imbalance of MMIs affects the switch performances. Finally, we make our concluding statements in Section VI.

II. Switch Architecture

A. 4 × 4 GMZI Switch

Fig. 1(a) shows the schematic of a typical 4 × 4 GMZI. Two identical 4×4 MMIs are used as the optical power splitter and combiner, which are connected by four waveguides each incorporating a phase shifter. This kind of structure can be used for either power splitting or switching depending on the phase shifts applied to the waveguide array [24]. The output of the GMZI is related to the input by multiplication of transfer matrices:

$$\begin{pmatrix} E_1^{out} \\ E_2^{out} \\ E_3^{out} \\ E_4^{out} \end{pmatrix} = M_c^{4\times4} M_\phi^{4\times4} M_c^{4\times4} \begin{pmatrix} E_1^{in} \\ E_2^{in} \\ E_3^{in} \\ E_4^{in} \end{pmatrix} \quad (1)$$

Manuscript received July 21, 2014; revised October 9, 2014 and November 25, 2014; accepted November 26, 2014. Date of publication December 9, 2014; date of current version February 20, 2015. This work was supported in part by the 973 Program (ID2011CB301700), the 863 Program (2013AA014402), the National Natural Science Foundation of China (61127016, 61107041, 61422508) and SRFDP of MOE under Grant 20130073130005.

The authors are with the State Key Laboratory of Advanced Optical Communication Systems and Networks, Department of Electronic Engineering, Shanghai Jiao Tong University, Shanghai 200240, China (e-mail: luliangjun@sjtu.edu.cn; ljzhou@sjtu.edu.cn; shulin.li@sjtu.edu.cn; xiangzi_sjtu@sjtu.edu.cn; lixinwan@sjtu.edu.cn; jpchen62@sjtu.edu.cn).

Color version of one or more of the figures in this paper are available online at uri http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JLT.2014.2376933

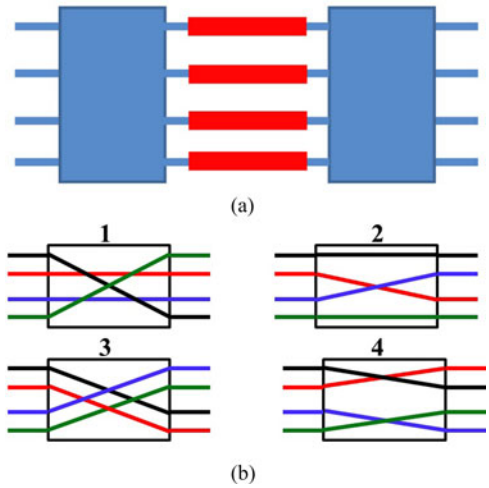

Fig. 1. (a) Schematic of a typical 4×4 GMZI. (b) Four switching states of the 4×4 GMZI switch.

TABLE I
PHASE RELATIONSHIPS OF THE 4×4 GMZI

Switching state	ϕ_1	ϕ_2	ϕ_3	ϕ_4
1	$\pi/2$	0	0	$\pi/2$
2	0	$\pi/2$	$\pi/2$	0
3	0	π	0	π
4	0	0	π	π

where E_i^{out} and E_i^{in} $(i = 1, 2, 3, 4)$ are the complex electric fields at the output and input ports, respectively, $M_\phi^{4\times4}$ is the phase modulation of the GMZI, and $M_c^{4\times4}$ is the transfer matrix of the 4 × 4 MMIs. $M_\phi^{4\times4}$ can be expressed as:

$$M_\phi^{4\times4} = \begin{bmatrix} e^{(i\phi_1)} & 0 & 0 & 0 \\ 0 & e^{(i\phi_2)} & 0 & 0 \\ 0 & 0 & e^{(i\phi_3)} & 0 \\ 0 & 0 & 0 & e^{(i\phi_4)} \end{bmatrix} \quad (2)$$

where ϕ_i is the phase shift of the *i*th waveguide, and $M_c^{4\times4}$ can be expressed as [24]:

$$M_c^{4\times4} = \frac{1}{2}\begin{bmatrix} 1 & -1/r & 1/r & 1 \\ -1/r & 1 & 1 & 1/r \\ r & 1 & 1 & -r \\ 1 & r & -r & 1 \end{bmatrix} \quad (3)$$

where $r = e^{(i\pi/4)}$ and the constant phase offset has been omitted without loss of generality.

When one connection is specified, all the other three connections for that switching state are uniquely determined. Therefore, the phases of the 4 arms can be solved given the connection of input port 1 to one of the output ports. The 4 × 4 GMZI has only 4 switching states denoted as "1", "2", "3", and "4" in Fig. 1(b). The phase relationships of the four states are listed in Table I.

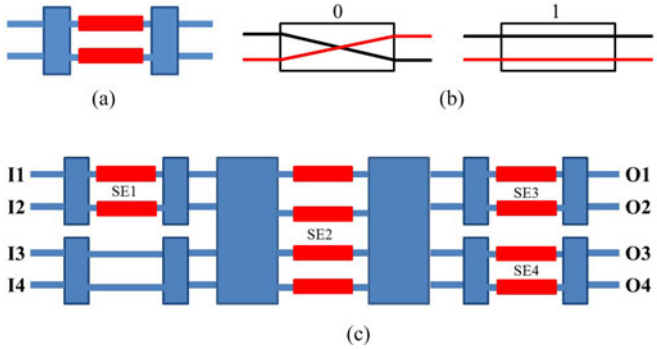

Fig. 2. (a) Schematic of a 2×2 MZI switch element. (b) "Cross" and "bar" states of the 2×2 MZI. (c) Schematic of the 4×4 non-blocking switch. The four active switch elements are labeled as "SE1", "SE2", "SE3", and "SE4".

B. 4 × 4 Non-Blocking GMZI Switch

As one 4 × 4 GMZI only has four switching states, it is incapable to form a 4 × 4 non-blocking switch with 24(= 4!) switching states. To provide the complete connections, we cascade the GMZI with 2 × 2 MZIs at the input and output ends. The 2 × 2 MZI consists of two 2 × 2 MMIs connected by two phase shifters, which is essentially the simplest version of GMZI, as shown in Fig. 2(a). By changing the phase difference of the two arms from 0 to π, the MZI is switched from the "cross" to the "bar" state corresponding to the "0" and "1" switching states, respectively, as illustrated in Fig. 2(b). Cascading three 2 × 2 MZIs to the 4 × 4 GMZI can already generate $4 \times 2 \times 2 \times 2 = 32$ permutations, covering the 24 essential states needed for non-blocking switching. Fig. 2(c) shows the topology of the 4 × 4 non-blocking switch. Note that we add one more passive 2 × 2 MZI without phase shifters at the input end in order to balance the switch architecture. Each routing path from an input port to an output port passes two 4 × 4 MMIs and four 2 × 2 MMIs. Table II lists the 24 permutations, the switching states of the 4 switch elements, and the power consumption.

III. DEVICE STRUCTURE AND FABRICATION

The waveguides in the switch have a width of 500 nm. They are tapered to 1.2 μm in a 10-μm-length before connecting with the MMIs in order to reduce the transmission loss. The 2 × 2 MMIs are 5 μm wide and 29.7 μm long, and the 4 × 4 MMIs are 12 μm wide and 269.3 μm long. The device is optimized for transverse electric (TE) polarization using the three-dimensional beam propagation method (BPM). Phase shifters based on silicon resistive microheaters are integrated in all switching elements. Phase shift can also be realized via the free carrier plasma dispersion (FCD) effect. Although it is faster and more power efficient than the TO effect, the accompanied free carrier absorption, however, inevitably brings about additional loss. As a result, the crosstalk due to unbalanced interference of MZI will increase [7]–[9]. Hence, we used the TO effect to design our device. Fig. 3(a) shows the cross-sectional view of the silicon resistive microheaters. The design detail of the microheater can be found in [26]. The length of the phase shifters is 400 μm. The

TABLE II
OPERATION STATES AND POWER CONSUMPTION OF THE 4 × 4 NON-BLOCKING SWITCH

State ID	O1	O2	O3	O4	SE1	SE2	SE3	SE4	Power (mW)
1	I3	I1	I2	I4	0	1	1	0	35.8
2	I3	I1	I4	I2	0	1	1	1	62.8
3	I1	I3	I2	I4	0	1	0	0	62.7
4	I1	I3	I4	I2	0	1	0	1	89.7
5	I3	I2	I1	I4	1	1	1	0	56.8
6	I3	I2	I4	I1	1	1	1	1	83.8
7	I2	I3	I1	I4	1	1	0	0	83.7
8	I2	I3	I4	I1	1	1	0	1	110.7
9	I2	I4	I3	I1	0	2	1	0	84.5
10	I2	I4	I1	I3	0	2	1	1	111.5
11	I4	I2	I3	I1	0	2	0	0	111.4
12	I4	I2	I1	I3	0	2	0	1	138.4
13	I1	I4	I3	I2	1	2	1	0	104.9
14	I1	I4	I2	I3	1	2	1	1	131.9
15	I4	I1	I3	I2	1	2	0	0	131.8
16	I4	I1	I2	I3	1	2	0	1	158.8
17	I4	I3	I1	I2	0	3	1	0	115.9
18	I4	I3	I2	I1	1	3	1	0	90.4
19	I3	I4	I2	I1	1	3	0	0	117.3
20	I3	I4	I1	I2	1	3	0	1	144.3
21	I2	I1	I4	I3	0	4	0	0	145.2
22	I2	I1	I3	I4	0	4	0	1	172.2
23	I1	I2	I4	I3	1	4	0	0	121.9
24	I1	I2	I3	I4	1	4	0	1	148.9

O*i* and I*i* ($i = 1, 2, 3, 4$) are the output and input ports of the 4×4 non-blocking switch, respectively. SE*i* ($i = 1, 2, 3, 4$) is the switch element as labeled in Fig. 2(c). SE1, SE3 and SE4 have 2 switching states: "0" and "1", and SE2 has 4 switching states: "1", "2", "3", and "4".

ridge waveguide has a high resistivity working as a microheater, so heat is generated inside the waveguide and directly interacts with the optical mode. Compared to conventional metallic heaters, it has higher tuning efficiency and faster temporal response [27]. The waveguide region in the heater is lightly N^- doped for low voltage operation while the free carriers induced absorption loss is negligible [26].

The device was fabricated on a silicon-on-isolator (SOI) wafer with a top silicon layer thickness of 220 nm and a buried oxide layer thickness of 2 μm. 248-nm deep ultra-violet photolithography was used to pattern the waveguides, and plasma dry etching was used to etch ∼160 nm of the top silicon layer. Subsequently, ion implantation of phosphorus was used to form the N^- doped regions with a doping concentration of 8×10^{16} cm^{-3}, and the N^+ doped regions with a concentration of $\sim 10^{20}$ cm $^{-3}$ for ohmic contact. Rapid thermal annealing at 1030° for 5 sec was used after ion implantation. After that, a 1.5 μm thick oxide was deposited as the upper cladding layer on the waveguide by using the plasma-enhanced chemical vapor deposition. Finally, contact holes were etched and aluminum connection was formed by sputtering and dry etching. The whole fabrication was carried out using a CMOS compatible process.

Fig. 3(b) shows the optical microscope image of the fabricated 4 × 4 switch. The footprint of the device is 2.8 × 0.65 mm^2, which is mainly resulted from the 400-μm-long phase shifters and 160×160 μm^2 electrical pads with a separation of 60 μm (limited by our wire-bonding machine). The device footprint can be reduced by designing shorter phase shifters and smaller wire-bonding pads. Grating couplers with a 630 nm period and a 70 nm shallow etch depth are used for input and output coupling. It should be noted that in our design we insert a directional coupler in each output waveguide so that light can be coupled out of the chip from both the left side (fiber array coupling) and the right side (individual fiber coupling) for easy testing. The directional coupler is designed to have a gap of 200 nm and a coupling length of 13 μm. The splitting loss at the fiber array end is about 4.8 dB based on the finite-difference time-domain simulation. The electrical pads were wire-bonded to a printed circuit board (PCB). Fig. 3(c) shows the image of the switch chip attached to a PCB with Au wire-bonding.

IV. EXPERIMENTS

A. Switch Characteristics

The switching performance of the device was characterized at 1532.2 nm wavelength, instead of 1550 nm, due to the fabrication deviation as will be explained in Section V. Light was launched to one input port, and a routing path from the input port to a specific output port was set up by applying proper voltages on all switch elements. We measured the transmitted optical power from this path by a power meter to obtain the device loss. The ratio of the input optical power to the output power is defined as fiber-to-fiber loss of the light path. Apart from the main path, the optical power is also partially coupled to the other three output ports, leading to crosstalk. For each switching state, we measured the loss and crosstalk of the four optical paths. The TO power consumptions of all 24 switching states are listed in Table II with the average being 109 mW, which can be further reduced by, e.g., using air trenches around the phase shifters [28]. The varied power consumption among all the 24 states is due to the different phase shifts required in each switching state as well as the random phase errors due to imperfect fabrication.

Fig. 4 shows the measured fiber-to-fiber losses of all the 24 states of the device. The coupling loss per facet is 9.6 dB at 1532.2 nm, which is estimated by measuring a straight waveguide with the same grating couplers. The large coupling loss is mainly attributed to the uniform grating design centered at 1550 nm wavelength with a 1 dB bandwidth of 17 nm. The coupling efficiency can be improved by nonuniform grating design [29]. An extra splitting loss of about 4.8 dB brought by the directional couplers is included in the transmission loss. The average on-chip insertion loss of the switch is hence 9 dB, with a variance of ±2 dB. The losses are mainly from the four 2 × 2 MMIs and two 4 × 4 MMIs. We attribute the variation of on-chip insertion loss to the difference in coupling efficiency of grating couplers and the unequal power splitting of the six MMIs. The on-chip insertion loss of the switch can be further reduced by optimizing the MMIs.

The crosstalk induced by the input port m ($m \neq i$) to the routing path I*i*-O*j* (*i, j* $= 1, 2, 3,$ and 4), is defined as the ratio of the leaked output power, $P_{\mathrm{out}(m \to j)}$, to the output power, $P_{\mathrm{out}(i \to j)}$ [17], [22]. One may note that there are different definitions of crosstalk [6], [30]. We use the above definition to favor fair comparison with other similar works. According to

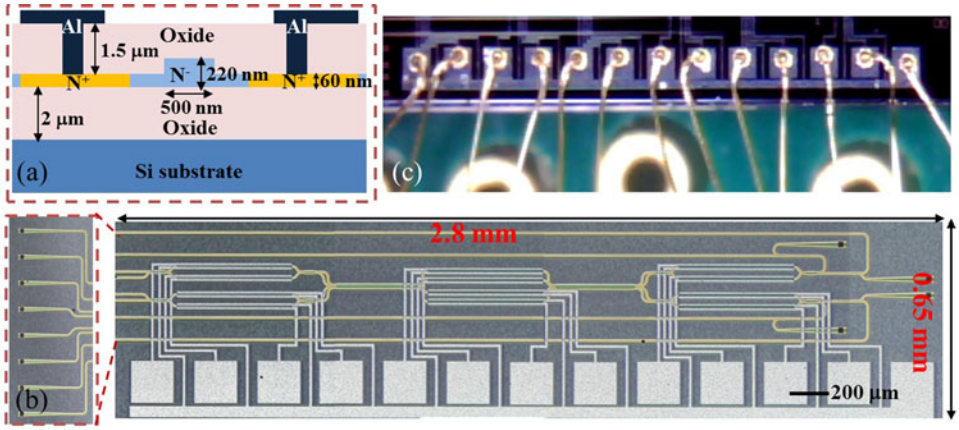

Fig. 3. (a) Cross-sectional schematic of the silicon resistive microheaters. (b) Optical microscope image of the 4×4 non-blocking switch with input and output waveguides all routed to the left side for fiber array coupling. (c) Image of the 4×4 switch after wire-bonding to a PCB.

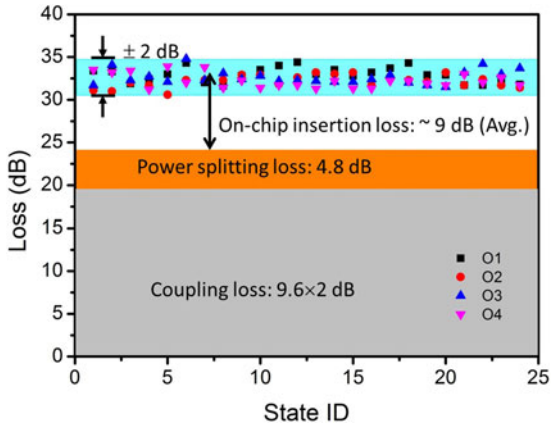

Fig. 4. Measured fiber-to-fiber loss of all 24 switching states of the 4×4 switch.

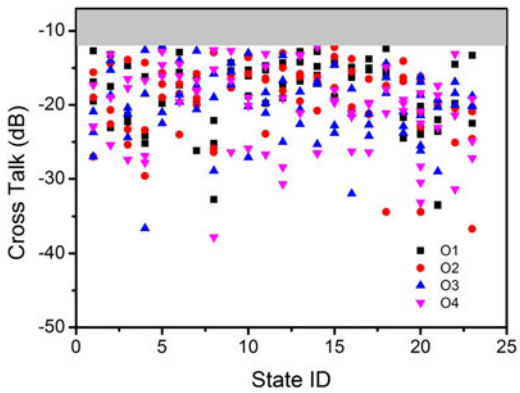

Fig. 5. Measured crosstalk of all 24 switching states of the 4×4 switch.

the definition, the leaked power for one specific routing path may come from three other input ports, so there are totally 12 crosstalk values for a switching state. The worst crosstalk of all the routing paths is defined as the switch crosstalk.Fig. 5 shows the crosstalk of all switching states at 1532.2 nm wavelength, where the crosstalk for each state is categorized into four groups according to the output ports. From the graph, the switch crosstalk is −12 dB, mainly resulted from the power imbalance of MMIs. In the next section, we will establish a theoretical model to investigate the influence of power imbalance on the switch crosstalk.

Table III compares our 4 × 4 switch with other GMZI-based optical switches demonstrated on various platforms. We note that the performance of our device is extracted by measuring all the 24 switching states. The power consumption of our device is high because we use TO effect rather than FCD effect for tuning. Silica-based PLC switches present very low crosstalk. However, they require even larger driving power.

Fig. 6 shows the measured transmission spectra of the switch for switching states #2, #14, #17 and #24, which cover the complete four switching states of the central 4 × 4 GMZI. As the two outer arms of the 4 × 4 GMZI are 56 μm longer than the inner arms, the spectra exhibit periodic interference patterns with a free-spectral-range (FSR) of 11.3 nm. The interference pattern can essentially be eliminated by designing a balanced waveguide array.

B. High-Speed QPSK Data Transmission

In order to verify the routing function of the 4 × 4 non-blocking switch, we performed optical data transmission experiments using high-speed QPSK optical signals. The experimental setup is shown in Fig. 7. A continuous wave (CW) light at 1532.2 nm wavelength is generated by a tunable laser source, and subsequently modulated by a $LiNbO_3$ based IQ modulator to generate the QPSK signal. The modulator is driven by two 20 Gb/s $2^{31}-1$ pseudo-random bit sequence radio frequency signals from a pulse-pattern generator, so the optical signal bit rate is 40 Gb/s. The optical signal is amplified by an erbium-doped fiber amplifier (EDFA) followed by a polarization controller to set the TE polarization before it is coupled into the chip by grating couplers. In order to compensate the loss of the device, the output optical signal is amplified by another EDFA followed by a band-pass filter to suppress the amplified spontaneous emission

TABLE III
COMPARISON OF GMZI-BASED SWITCHES

Technologies	Port numbers	Blocking characteristics	Insertion loss (dB)	Crosstalk (dB)	Power consumption
GaAs/AlGaAs [17]	10×10	Blocking	12.2	−10	12.4 V/ 2π [1]
InGaAsP/InP [18]	1×4	Non-blocking	Not mentioned	−14.47	Not mentioned
Silica PLC [20]	8×8	Non-blocking	6	−34	290 mW/π [1]
Silica PLC [21]	4×4	Non-blocking	2.8	−35	Not mentioned
SOI [22]	1×4	Non-blocking	1.7	−11.38	31.7 mW [2]
SOI [23]	3×3	Blocking	Not mentioned	−11.1	97.5 mW [3]
SOI [this work]	4×4	Non-blocking	9	−12	109 mW [2]

[1] : voltage or power needed for 2π or π phase shift; [2] : average power consumption; [3] : maximum power consumption.

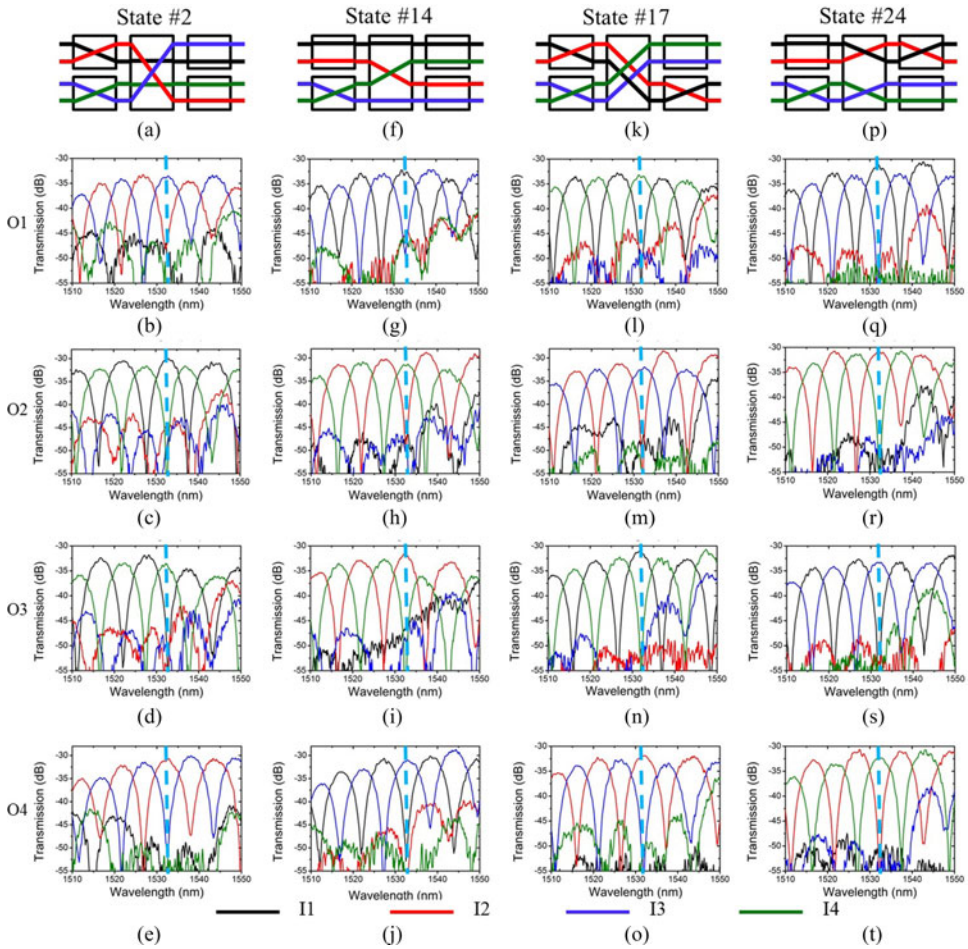

Fig. 6. Four typical switching states and their corresponding transmission spectra of the 4 × 4 switch. (a)-(e): State #2; (f)–(j) State #14; (k)–(o): State #17; (p)–(t) State #24.

noise from the EDFAs. A variable optical attenuator is used to adjust the optical power before the optical signal is received and analyzed by an optical modulation analyzer (Agilent, N4392A). The error-vector-magnitude (EVM) and the bit error rate (BER) are obtained from the measured constellation diagrams.

We measured the optical signal transmission for switching states #2, #14, #17 and #24. Fig. 8(a) shows the constellation diagram of the system back-to-back (BtB) transmission, with an EVM and a BER of 13.0% and 8.2×10^{-15}, respectively. Figs. 8(b)–8(e) depict the constellation diagrams of the four output ports. The measured EVMs are all smaller than 13.9%, indicating the signal is degraded by less than 1% after passing through the device. The BERs of the measured 16 paths are degraded by less than 2 orders compared to the BtB transmission. Therefore, our 4 × 4 switch is capable of switching 40 Gb/s QPSK signal with high signal quality, even though it has a relatively high insertion loss.

V. DISCUSSIONS

We use a heuristic model based on transfer matrix and random error statistics to estimate the crosstalk of the 4 × 4 switch [22].

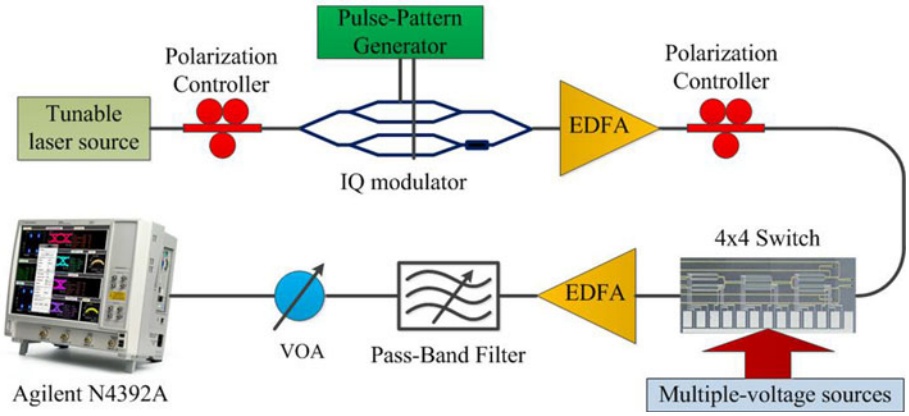

Fig. 7. System setup for optical signal transmission through the 4×4 switch.

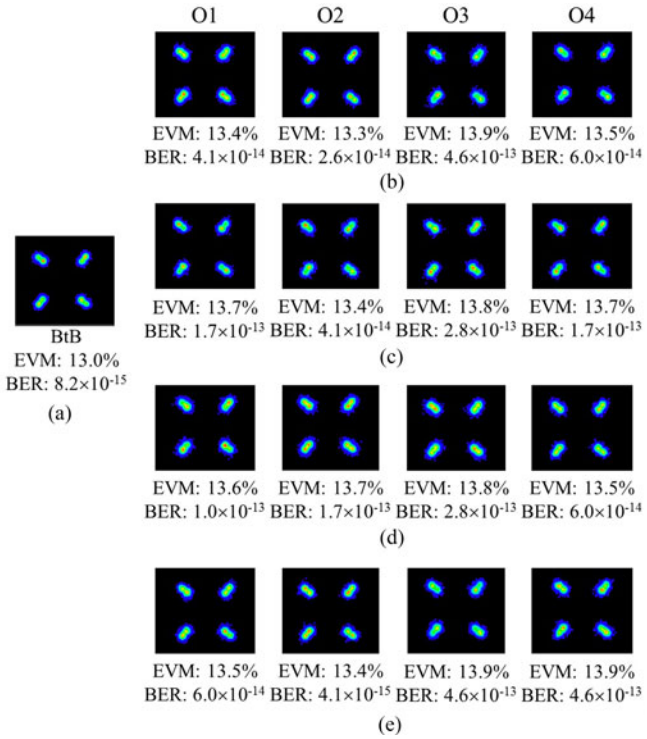

Fig. 8. Measured constellation diagrams of a 40 Gb/s QPSK signal. (a) Back-to-back transmission; (b) State #2; (c) State #14; (d) State #17; (e) State #24.

As the loss of MMIs only affects the insertion loss of the 4 × 4 switches, the power imbalance of the 2 × 2 and 4 × 4 MMIs is the main source for the deterioration of switch crosstalk. Here the power imbalance of a MMI is defined as the power ratio between the highest and the lowest powers at the output ports. We neglect the losses of the MMIs and only consider the effect of power imbalance on device performances. Random values between 0 and 1 are used to represent simulation and fabrication uncertainties, while two variables $\sigma_m^{2\times2}$ and $\sigma_m^{4\times4}$ are used to represent the largest power imbalance of the 2×2 and 4×4 MMIs, respectively. Considering both amplitude and phase variations, the elements $M_{n,l}^{2\times2}$, $M_{n,l}^{4\times4}$ in the transfer matrices of the 2 × 2 and 4 × 4 MMIs are written as:

$$M_{n,l}^{2\times2} = \frac{\sqrt{2}}{2}\left[1-\sigma_M^{2\times2}rand()\right]\exp\left\{i\left[\psi_{n,l}^{2\times2} + \sigma_M^{2\times2}\left(rand()-\frac{1}{2}\right)\right]\pi\right\} \quad (4)$$

$$M_{n,l}^{4\times4} = \frac{1}{2}\left[1-\sigma_M^{4\times4}rand()\right]\exp\left\{i\left[\psi_{n,l}^{4\times4} + \sigma_M^{4\times4}\left(rand()-\frac{1}{2}\right)\right]\pi\right\} \quad (5)$$

where $\psi_{n,l}^{2\times2}$ and $\psi_{n,l}^{4\times4}$ are the ideal phases of the 2×2 and 4×4 MMIs, respectively. By using the transfer matrix method, the output matrix M_{trans} of the 4 × 4 switch is given by

$$\begin{aligned} M_{trans} &= M_{out}^{2\times2}\cdot M_{mid}^{4\times4}\cdot M_{in}^{2\times2} \\ &= diag(M_c^{2\times2}, M_c^{2\times2})\cdot M_{\phi1}^{2\times2} diag(M_c^{2\times2}, M_c^{2\times2}) \\ &\quad \cdot M_c^{4\times4} M_\phi^{4\times4} M_c^{4\times4} \\ &\quad \cdot diag(M_c^{2\times2}, M_c^{2\times2})\cdot M_{\phi2}^{2\times2}\cdot diag(M_c^{2\times2}, M_c^{2\times2}) \end{aligned} \quad (6)$$

where $M_c^{2\times2}$ is the transfer matrix of the 2×2 MMIs, $M_{\phi i}^{2\times2}(i = 1, 2)$ and $M_\phi^{4\times4}$ represent the phase modulation of the 2×2 and 4×4 switch elements, respectively.

With the phases of all the switch elements set for a certain switching state, the crosstalk of each routing path can be derived by Eq. (6). As defined, the worst one is the switch crosstalk. We repeated the above process 1000 times with random power ratio fluctuations and calculated the average value of the crosstalk. The result is shown in Fig. 9. In practice, it is relatively easier to control the power imbalance of 2 × 2 MMIs than that of 4×4 MMIs. Therefore, we used a smaller scale for 2 × 2 MMIs than that for 4 × 4 MMIs in Fig. 9. From the contour plot, one can see that, in order to achieve a crosstalk below −20 dB, the power imbalance of the 2 × 2 and 4 × 4 MMIs must be smaller than 0.8 and 0.5 dB, respectively.

As BPM with the slowly-varying envelope approximation is not accurate enough to simulate the high index contrast silicon

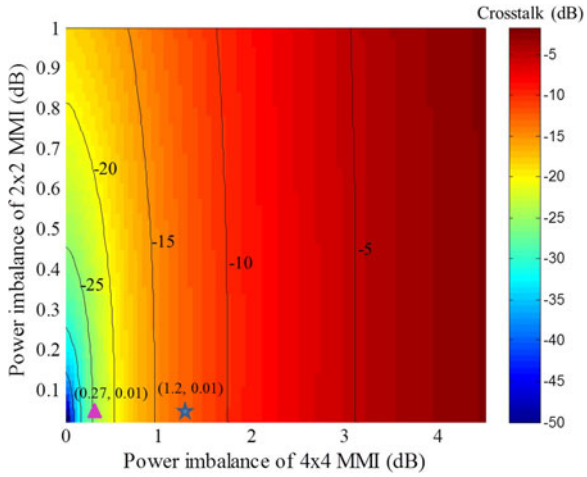

Fig. 9. Tolerance analysis of power imbalance of the 4 × 4 and 2 × 2 MMIs on the crosstalk of the device. The asterisk represents the simulation of our fabricated device and the triangle represents the targeted design to lower crosstalk.

waveguides [31], the 2 × 2 and 4 × 4 MMIs designed using BPM incur certain power imbalance. Using the eigenmode expansion (EME) method which is more accurate in solving the Maxwell's equations [32], we obtain the power imbalance of our 2 × 2 and 4 × 4 MMIs to be 0.01 and 1.2 dB, respectively. This leads to about −12.5 dB crosstalk according to our model as shown in Fig. 9, which is in good agreement with the experiment. Based on the EME, it is possible to further optimize the design of 4 × 4 MMI and reduce the power imbalance to 0.27 dB, which as a result will give a crosstalk of better than −25 dB according to Fig. 9.

VI. Conclusion

We have designed, fabricated, and experimentally demonstrated a 4 × 4 silicon TO non-blocking switch based on MMI. The switch architecture is present and the non-blocking characteristic is analyzed. Experimental results show that the average on-chip insertion loss of the 24 states is within 9 ± 2 dB at 1532.2 nm, the crosstalk is better than −12 dB, and the average power consumption of all 24 states is 109 mW. Optical transmission spectra show periodic interference patterns with a FSR of 11.3 nm due to the unbalanced waveguide array design. We conducted optical signal transmission experiments using a high-throughput 40 Gb/s QPSK signal and no significant deterioration was observed on constellation diagrams. We also studied the influence of power imbalance of MMIs on switch crosstalk by using the transfer matrix method. The performance of the 4 × 4 optical switch can be further improved by reducing the loss and improving the power splitting uniformity of the 4 × 4 and 2 × 2 MMIs.

Acknowledgment

The authors acknowledge IME Singapore for device fabrication.

References

[1] S. J. B. Yoo, "Optical packet and burst switching technologies for the future photonic internet," *J. Lightw. Technol.*, vol. 24, no. 12, pp. 4468–4492, Dec. 2006.

[2] A. Biberman and K. Bergman, "Optical interconnection networks for high-performance computing systems," *Rep. Prog. Phys.*, vol. 75, p. 046402 (15 pages), Mar. 2012.

[3] R. G. Beausoleil, M. McLaren, and N. P. Jouppi, "Photonic architectures for high-performance data centers," *IEEE J. Sel. Top. Quantum Electron.*, vol. 19, no. 2, pp. 3700109–3700117, Mar./Apr. 2013.

[4] L. Chen and Y. K. Chen, "Compact, low-loss and low-power 8×8 broadband silicon optical switch," *Opt. Exp.*, vol. 20, pp. 18977–18985, Aug. 2012.

[5] B. G. Lee, A. V. Rylyakov, W. M. J. Green, S. Assefa, C. W. Baks, R. Rimolo-Donadio, D. M. Kuchta, M. H. Khater, T. Barwicz, C. Reinholm, E. Kiewra, S. M. Shank, C. L. Schow, and Y. A. Vlasov, "Monolithic silicon integration of scaled photonic switch fabrics, CMOS logic, and device driver circuits," *J. Lightw. Technol.*, vol. 32, no. 4, pp. 743–751, Feb. 2014.

[6] K. Suzuki, K. Tanizawa, T. Matsukawa, G. Cong, S. H. Kim, S. Suda, M. Ohno, T. Chiba, H. Tadokoro, M. Yanagihara, Y. Igarashi, M. Masahara, S. Namiki, and H. Kawashima, "Ultra-compact 8 × 8 strictly-non-blocking Si-wire PILOSS switch," *Opt. Exp.*, vol. 22, pp. 3887–3894, Feb. 2014.

[7] J. Xing, Z. Li, P. Zhou, X. Xiao, J. Yu, and Y. Yu, "Nonblocking 4×4 silicon electro-optic switch matrix with push–pull drive," *Opt. Lett.*, vol. 38, pp. 3926–3929, Oct. 2013.

[8] M. Yang, W. M. J. Green, S. Assefa, J. Van Campenhout, B. G. Lee, C. V. Jahnes, F. E. Doany, C. L. Schow, J. A. Kash, and Y. A. Vlasov, "Non-blocking 4×4 electro-optic silicon switch for on-chip photonic networks," *Opt. Exp.*, vol. 19, pp. 47–54, Dec. 2010.

[9] J. Xing, Z. Li, Y. Yu, and J. Yu, "Low cross-talk 2 × 2 silicon electro-optic switch matrix with a double-gate configuration," *Opt. Lett.*, vol. 38, pp. 4774–4776, Nov. 2013.

[10] P. Dasmahapatra, R. Stabile, A. Rohit, and K. A. Williams, "Crossbar switch matrix using fifth-order resonators," in *Proc. 10th Int. Conf. Group IV Photon.*, 2013, pp. 11–12.

[11] N. Sherwood-Droz, H. Wang, L. Chen, B. G. Lee, A. Biberman, K. Bergman, and M. Lipson, "Optical 4×4 hitless silicon router for optical networks-on-chip (NoC)," *Opt. Exp.*, vol. 16, pp. 15915–15922, Sep. 2008.

[12] R. Q. Ji, J. Xu, and L. Yang, "Five-port optical router based on microring switches for photonic networks-on-chip," *IEEE Photon. Technol. Lett.*, vol. 25, no. 5, pp. 492–495, Mar. 2013.

[13] M. Bachmann, P. A. Besse, and H. Melchior, "General self-imaging properties in N x N multimode interference couplers including phase relations," *Appl. Opt.*, vol. 33, pp. 3905–3911, Jun. 1994.

[14] N. S. Lagali, M. R. Paiam, R. I. MacDonald, K. Worhoff, and A. Driessen, "Analysis of generalized Mach–Zehnder interferometers for variable-ratio power splitting and optimized switching," *J. Lightw. Technol.*, vol. 17, no. 12, pp. 2542–2550, Dec. 1999.

[15] L. W. Cahill, "The synthesis of generalized Mach–Zehnder optical switches based on multimode interference (MMI) couplers," *Opt. Quantum Electron.*, vol. 35, pp. 465–473, 2003.

[16] L. Cahill, "Optical switching using cascaded generalized Mach–Zehnder switches," in *Proc. TENCON IEEE Region 10*, 2005, pp. 1–5.

[17] R. M. Jenkins, J. M. Heaton, D. R. Wight, J. T. Parker, J. C. H. Birbeck, G. W. Smith, and K. P. Hilton, "Novel 1×N and N×N integrated optical switches using self-imaging multimode GaAs/AlGaAs waveguides," *Appl. Phys. Lett.*, vol. 64, pp. 684–686, 1994.

[18] S. Tomofuji, S. Matsuo, T. Kakitsuka, and K. Kitayama, "Dynamic switching characteristics of InGaAsP/InP multimode interference optical waveguide switch," *Opt. Exp.*, vol. 17, pp. 23380–23388, Dec. 2009.

[19] J. M. Heaton, R. M. Jenkins, D. R. Wight, J. T. Parker, J. C. H. Birbeck, and K. P. Hilton, "Novel 1-to-N way integrated optical beam splitters using symmetric mode mixing in GaAs/AlGaAs multimode waveguides," *Appl. Phys. Lett.*, vol. 61, pp. 1754–1756, 1992.

[20] M. P. Earnshaw, J. B. D. Soole, M. Cappuzzo, L. Gomez, E. Laskowski, and A. Paunescu, "8 × 8 optical switch matrix using generalized Mach–Zehnder interferometers," *IEEE Photon. Technol. Lett.*, vol. 15, no. 6, pp. 810–812, Jun. 2003.

[21] M. P. Earnshaw, J. B. D. Soole, M. Cappuzzo, L. Gomez, E. Laskowski, and A. Paunescu, "Compact, low-loss 4 × 4 optical switch matrix using multimode interferometers," *Electron. Lett.*, vol. 37, pp. 115–116, 2001.

[22] H. Zhou, J. Song, E. K. S. Chee, C. Li, H. Zhang, and G. Lo, "A compact thermo-optical multimode-interference silicon-based 1×4 nano-photonic switch," *Opt. Exp.*, vol. 21, pp. 21403–21413, Sep. 2013.
[23] W. Wang, H. Zhou, J. Yang, M. Wang, and X. Jiang, "Highly integrated 3×3 silicon thermo-optical switch using a single combined phase shifter for optical interconnects," *Opt. Lett.*, vol. 37, pp. 2307–2309, Jun. 2012.
[24] L. W. Cahill, "The modeling of integrated optical power splitters and switches based on generalized Mach–Zehnder devices," *Opt. Quantum Electron.*, vol. 36, pp. 165–173, 2004.
[25] N. S. Lagali, I. MacDonald, and R. Paiam, "N× N non-blocking optical switch," U.S. Patent 6 292 597, Sep. 18, 2001.
[26] L. Lu, L. Zhou, X. Li, and J. Chen, "Low-power 2×2 silicon electro-optic switches based on double-ring assisted Mach–Zehnder interferometers," *Opt. Lett.*, vol. 39, pp. 1633–1636, Mar. 2014.
[27] L. Zhou, X. Zhang, L. Lu, and J. Chen, "Tunable vernier microring optical filters with p-i-p type microheaters," *IEEE Photon. J.*, vol. 5, no. 4, pp. 6601211–6601221, Aug. 2013.
[28] P. Dong, W. Qian, H. Liang, R. Shafiiha, D. Feng, G. Li, J. E. Cunningham, A. V. Krishnamoorthy, and M. Asghari, "Thermally tunable silicon racetrack resonators with ultralow tuning power," *Opt. Exp.*, vol. 18, pp. 20298–20304, Sep. 2010.
[29] L. He, Y. Liu, C. Galland, A. E.-J. Lim, G.-Q. Lo, T. Baehr-Jones, and M. Hochberg, "A high-efficiency nonuniform grating coupler realized with 248-nm optical lithography," *IEEE Photon. Technol. Lett.*, vol. 25, no. 14, pp. 1358–1361, Jul. 2013.
[30] R. Ji, L. Yang, L. Zhang, Y. Tian, J. Ding, H. Chen, Y. Lu, P. Zhou, and W. Zhu, "Microring-resonator-based four-port optical router for photonic networks-on-chip," *Opt. Exp.*, vol. 19, pp. 18945–18955, Sep. 2011.
[31] H. Zhou, J. Song, C. Li, H. Zhang, and P. G. Lo, "A library of ultra-compact multimode interference optical couplers on SOI," *IEEE Photon. Technol. Lett.*, vol. 25, no. 12, pp. 1149–1152, Jun. 2013.
[32] (2014). [Online]. Available: https://www.lumerical.com/tcad-products/mode/EME

Liangjun Lu received the B.S. degree from the Department of Optical Engineering, Zhejiang University, Hangzhou, China, in 2011. He is currently working toward the Ph.D. degree in electrical engineering at the State Key Laboratory of Advanced Optical Communication Systems and Networks, Shanghai Jiao Tong University, Shanghai, China. His research interest includes silicon optical switch.

Linjie Zhou (M'04) received the B.S. degree in microelectronics from Peking University, Beijing, China, in 2003. He received the Ph.D. degree in electronic and computer engineering from the Hong Kong University of Science and Technology, Hong Kong, in 2007. From 2007 to 2009, he worked as a Postdoctoral Researcher at the University of California, Davis, CA, USA. He is currently an Associate Professor at the State Key Laboratory of Advanced Optical Communication Systems and Networks, Shanghai Jiao Tong University, Shanghai, China. His research interests include silicon photonics, plasmonic waveguide devices, and photonic-integrated circuits.

Shulin Li received the B.S. and M.S. degrees in electrical engineering from Shanghai Jiao Tong University, Shanghai, China, in 2011 and 2014, respectively. Her current research interests include silicon optical switch and optical signal processing using silicon photonic devices.

Zuxiang Li received the B.S. degree in communication engineering from the Southwest University of Science and Technology, Mianyang, China, in 2013. He is currently a Graduate Student in the Department of Electrical Engineering, Shanghai Jiao Tong University, Shanghai, China. His current research interest includes package of silicon photonic devices.

Xinwan Li (SM'10) received the M.S. degree from Shanghai University, Shanghai, China, in 1993, and the Ph.D. degree from Shanghai Jiao Tong University, Shanghai, China, in 2005. Since 1993, he has been with Shanghai Jiao Tong University, where he is currently a Professor. From 1997 to 1998, he was with Essex University, Colchester, U.K., as a Research Assistant. In 2001, he joined OPCOM Inc. as an Engineer and became a Visiting Professor of Chonbuk National University in 2007. His main research interests include optical switching technologies and advanced optical fiber components. He is a Senior Member of the IEEE Photonics Society and the Chair of IEEE Communications Society Shanghai Chapter.

Jianping Chen received the B.S. degree from Zhejiang University, Hangzhou, China, in 1983, and the M.S. and Ph.D. degrees from Shanghai Jiao Tong University, Shanghai, China, in 1986 and 1992, respectively. He is currently a Professor with the State Key Laboratory of Advanced Optical Communication Systems and Networks, Department of Electronic Engineering, Shanghai Jiao Tong University. His main research interests include photonic devices and signal processing, optical networking, and sensing optics. He is also a Principal Scientist of 973 Project in China.