4 × 4 Silicon Optical Switches Based on Double-Ring-Assisted Mach–Zehnder Interferometers

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***Abstract*— We present the experimental demonstration of a 4 × 4 silicon electro-optic (EO) switch fabric based on a Benes architecture. Double-ring-assisted Mach–Zehnder interferometers (DR-MZIs) are utilized as the basic switch elements. Silicon resistive microheaters and p-i-n diodes are embedded in both of the microrings of the DR-MZIs for low-loss thermo-optic (TO) phase correction and high-speed switching operation, respectively. The TO tuning power dissipated to align all resonances is 22.37 mW. The maximum EO tuning power required to switch all DR-MZIs is only 1.38 mW. The average on-chip insertion loss is in the range of 4–5.8 dB for all switching states. The transmission spectrum measurement shows that the device can perform switching in a ∼35-GHz spectral window with the worst crosstalk being −18.4 dB.**

***Index Terms*— Optical switches, integrated optics, optical interconnections.**

I. Introduction

OPTICAL switches, which are implemented to establish reconfigurable connections between multiple sources and multiple destinations, are essential building blocks for both long-haul optical communications and short-reach photonic networks-on-chip [1]–[3]. Nowadays, the silicon-on-insulator (SOI) platform has attracted lots of attention for its high refractive index contrast and its compatibility with complementary metal-oxide-semiconductor (CMOS) technologies. Silicon electro-optic (EO) switches based on free-carrier plasma dispersion (FCD) effect have been considered as a viable solution for high-speed all-optical networks with a switching time in the order of nanosecond.

N × N optical switches are usually constructed by 1×2 or 2×2 switch elements with scalable switching architectures, such as Crossbar [4]–[6], Benes [7], [8], Switch-and-Select [9], path-independent insertion-loss (PILOSS) [10], [11]. Most of the switch elements are based on Mach-Zehnder interferometers (MZIs) [7]–[14] and microring resonators (MRRs) [5], [6], [15]–[17]. MZIs have a broadband spectral response. However, they require a phase shift of π to change the switching state, which suffers extra free-carrier absorption (FCA) loss for EO switching. Thus, it deteriorates the performance of MZIs with limiting crosstalks [14]. In contrast, single MRRs have a narrow optical bandwidth and a Lorentzian line shape of the passband. Although the refractive index detuning for MRR-based switches is much less than that of MZIs, FCA-induced loss decreases the Q-factor of MRRs, leading to a wider optical bandwidth and making the passband roll-off even slower. As a result, it needs a larger phase shift to achieve a low crosstalk [5].

Previously, we have demonstrated a 2 × 2 silicon EO switch element based on a double-ring assisted MZI (DR-MZI) [18]. As the DR-MZIs combine the merits of resonance enhancement in MRRs and the coherent interference in MZIs, they exhibit lower power consumption and crosstalk than MZIs and MRRs. In this letter, we experimentally demonstrate a 4×4 silicon non-blocking optical switch fabric consisting of six DR-MZIs in a Benes architecture. For all the six DR-MZIs, EO and thermo-optic (TO) tuning elements are imbedded in each MRR for fast switching operation and low-loss resonance alignment, respectively. The TO power consumption is 22.37 mW, while the maximum EO switching power is 1.38 mW. The footprint of the chip is 3.4×1.6 mm^2. The worst crosstalk of the device is −18.4 dB at 1555.62 nm wavelength. The average on-chip insertion loss is in the range of 4.0 dB to 5.8 dB.

II. Device Structure and Fabrication

Figure 1 shows the architecture of the 4×4 Benes switch fabric. It is a rearrangeable non-blocking switch. Compared with other switching architectures, Benes switches require the minimum number of switch elements to obtain the full switching states. Thus, switches with the Benes structure have the merits of lower power consumption and lower insertion loss. In a 4×4 switch, it only needs three stages of switch elements, which results in a total number of six switch elements. As can be seen, two waveguide crossings are necessary to construct the fabric. In order to reduce the insertion loss and the crosstalk at each crossing, we design 90°-crossed 1×1 MMIs based on the self-imaging principle for the light to cross over the waveguide junction.

The 2×2 DR-MZI switch element is composed of a symmetric MZI coupled to two identical MRRs, with one

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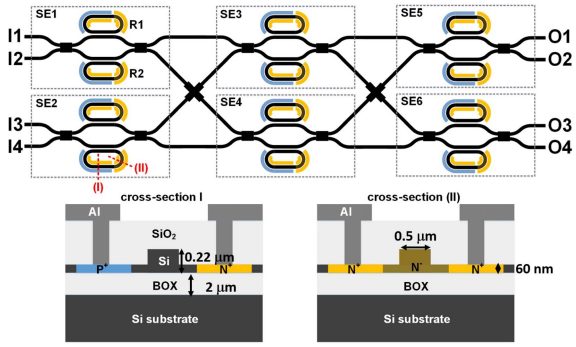

Fig. 1. 4×4 Benes switch architecture. Each switch element is based on a 2 × 2 DR-MZI. The cross-section views illustrate the structure of the p-i-n diode and the silicon resistive microheater. SE: the switch elements of the architecture, R1 and R2: the top and the bottom MRRs of the DR-MZI, respectively.

MRR on each arm. When the two MRRs are aligned at the same resonance wavelength, the phase difference between the two waveguide arms is 0, and the DR-MZI is at the cross state, which is notated as "0." The phase of over-coupled MRRs changes rapidly around a resonance, and thus, a slight variation in refractive index of one MRR can change the phase difference between the two arms to π. As a result, the switching state of the DR-MZI is flipped to the bar state, which is notated as "1." Therefore, the 2 × 2 DR-MZIs are more power-efficient than individual MZIs or MRRs, and the performance deterioration due to FCA is also alleviated. Because of fabrication errors, MRRs may not resonate at exactly the same wavelength. In order to align all resonances, we integrate a silicon resistive microheater in each MRR for phase-error correction. The microheater is made of a partial ring waveguide with light doping, allowing for low-loss and high- efficient TO tuning. Meanwhile, in order to realize fast switching, p-i-n diodes are also imbedded in both MRRs of the DR-MZI. It should be noted that in fact EO tuning of one MRR is enough for switching operation. The other EO tuner on the other MRR could work as a backup in the case of malfunction of the first one. The working principle and the design details of the 2×2 DR-MZI element can be found in our previous work [18].

The 4×4 switch was fabricated on a SOI wafer with a top silicon layer height of 220 nm and a buried oxide (BOX) layer thickness of 2 μm. The device is based on ridge waveguides with a waveguide width and a slab layer thickness of 500 nm and 60 nm, respectively. 248-nm deep ultraviolet (DUV) photolithography was employed to pattern the waveguides, and followed by plasma dry etching of the silicon. Subsequently, ion implantation of phosphorus and boron was used to form the N^- doped regions with a doping concentration of 8×10^{16} cm^{-3}, the N^+ and P^+ doped regions with a doping concentration of $\sim10^{20}$ cm^{-3}. Rapid thermal annealing at 1030°C for 5 seconds was used after ion implantation. After that, a 1.5-μm-thick oxide was deposited as the upper cladding layer on the waveguide by using the plasma-enhanced chemical vapor deposition (PECVD). Finally, contact holes were etched and aluminum was deposited to form metal connections. The whole fabrication process was done in IME Singapore using CMOS-compatible processes.

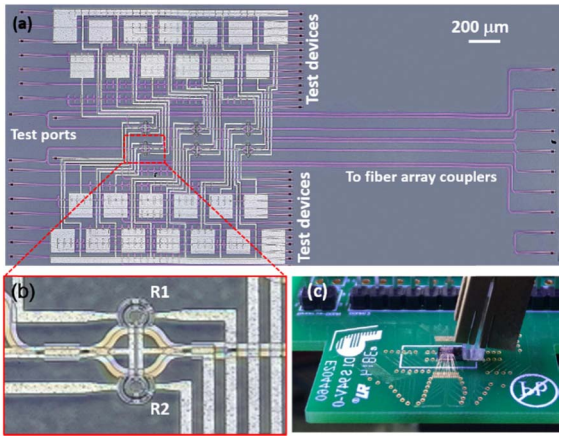

Fig. 2. (a) Microscope image of the fabricated switch. (b) Zoom-in image of the 2×2 DR-MZI. (c) Switch chip wire-bonded to a PCB. A fiber array is employed for light coupling on top of the chip.

Figure 2(a) shows the microscope image of the fabricated 4 × 4 switch chip. The footprint of the chip is 3.4 × 1.6 mm^2, including all the electrical pads and the fiber array coupling region. Grating couplers with a 630 nm period and a 70 nm shallow etch depth are used for coupling with optical fibers at the input and output ends. The input and output waveguides are elongated before terminated with grating couplers in order to leave enough space for fiber array coupling and wire-bonding of electrical pads. In our design, a directional coupler is used in each output waveguide to split and route light to both the right side (fiber array coupling) and the left side (single fiber coupling) for convenient chip testing and packaging. The directional coupler has a gap width of 200 nm and a coupling length of 13 μm. The power splitting loss for the fiber array end is about 6.2 dB around 1550 nm wavelength based on finite-difference time-domain (FDTD) simulations. Figure 2(b) shows the zoom-in view of the DR-MZI switch element. The 3-dB couplers in the MZIs are constructed by 2 × 2 multimode interferometers (MMIs) with a width and a length of 5 and 31.5 μm, respectively. The radius of MRRs is designed as 10 μm. The gap width between the MRR and the bus waveguide is 200 nm, and the coupling length is designed as 2.7 μm. The width and the length of the 1×1 MMIs in the waveguide crossings are 1.15 and 4.77 μm, respectively. The signal pads were wire-bonded to a printed circuit board (PCB) for electrical tuning of the silicon resistive microheaters and the p-i-n diodes. Figure 2(c) shows the photo of the switch chip after wire-bonding.

III. Experiments

The transmission spectrum of the switch was measured using the Agilent loss and dispersion analyzer (86038B). Transverse electrically (TE)-polarized light is coupled in and out of the chip via grating couplers. First, we characterize the power efficiency of the silicon resistive microheaters and the p-i-n diodes by extracting the resonance shift of a 2×2 DR-MZI switch element upon electrical tuning. Figures 3(a) and 3(b) show the cross-port transmission spectra of the 2×2 DR-MZI with voltages applied to the silicon resistive microheater and the p-i-n diode of one MRR, respectively.

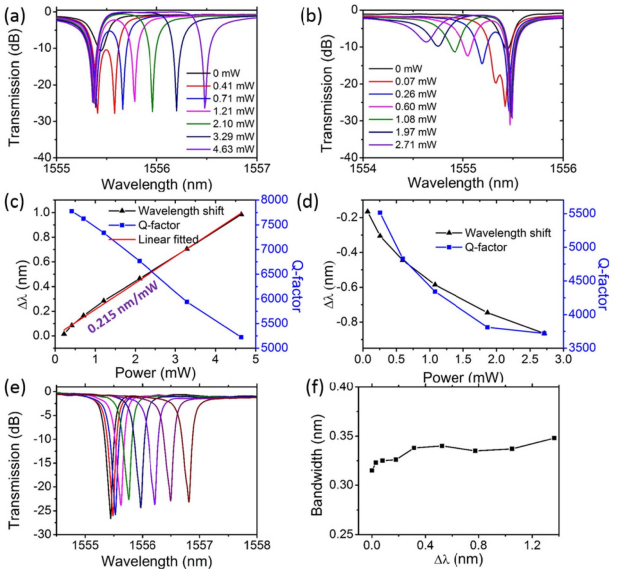

Fig. 3. (a) and (b) Measured cross-port transmission spectra of the 2×2 DR-MZI switch element with (a) TO tuning and (b) EO tuning of one MRR. (c) and (d) Resonance shift and Q-factor of the microring versus power consumption for (c) TO tuning and (d) EO tuning. (e) Measured cross port transmission spectra of the 2×2 DR-MZI at the bar state when the switch operational wavelength is tuned. (f) Extracted optical bandwidth versus wavelength shift.

As can be seen, the resonance red-shifts with its extinction ratio maintained upon TO tuning, while the resonance blue-shifts with a gradually decreased extinction ratio and Q-factor upon EO tuning due to the FCA effect. As for our 4×4 switch, the maximum resonance misalignment is about 0.8 nm. The switch performance is degraded dramatically if we only use EO tuning. Instead, TO tuning does not bring much extra loss, which is suitable for fabrication-error correction. Figures 3(c) and 3(d) show the resonance shift and Q-factor of the microring over TO and EO power consumption, respectively. By linear fitting, the TO tuning efficiency is extracted to be 0.215 nm/mW. The EO tuning efficiency decreases with tuning power, which is likely because of heat generation upon EO tuning. As can be seen, both the TO and EO tuning lead to the drop of the Q-factor. However, the Q-factor upon TO tuning is decreased more slowly than that upon EO tuning. We also measured the optical bandwidth of the 2×2 switch element when the operational wavelength is tuned a few wavelengths. It should be noted that, both of the microrings are TO-tuned in shifting the operational wavelength. Figure 3(e) shows the cross-port transmission spectra of the 2×2 DR-MZI at the bar state. The optical bandwidth is changed from 0.315 to 0.348 nm when the operational wavelength is shifted by ∼1.37 nm, as illustrated in Fig. 3(f).

Next, we present the measurement of the 4×4 switch. As the resonances of MRRs in all the DR-MZIs are not at the same wavelength due to fabrication errors, we first align the resonance wavelengths of all the 12 MRRs to the same wavelength by using the microheaters. In principle, the operational wavelength can be set to any wavelength as the TO tuner has a relatively large tuning range that covers one resonance free spectral range (FSR). Here, we choose one MRR resonance wavelength (1555.62 nm) as the operational

TABLE I
POWER CONSUMPTION OF THE 4×4 NON-BLOCKING SWITCH

	R1 (TO)	R2 (TO)	R1 (EO)
SE1 (mW)	1.094	1.708	0.223
SE2 (mW)	2.565	2.277	0.221
SE3 (mW)	2.086	3.916	0.197
SE4 (mW)	1.456	1.160	0.256
SE5 (mW)	0	3.335	0.259
SE6 (mW)	1.978	0.803	0.232

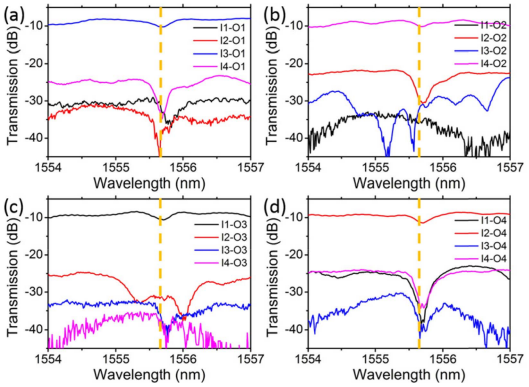

Fig. 4. Measured transmission spectra from all the four input ports to (a) O1, (b) O2, (c) O3, and (d) O4 of the switch at the "000000" state. The vertical dashed line is defined as the switch operational wavelength.

wavelength, and the other 11 MRRs are tuned to minimize the TO power consumption. Once the phase errors are all corrected, all the switch elements are at the cross state, which we refer to as "000000" state. The TO tuning powers of all the six DR-MZIs are listed in Table I. The minimum total TO power to correct fabrication errors is 22.37 mW. It should be noted that in practice the aligned wavelength may not be exactly the target operational wavelength. In this case, all the MRRs need to be thermally shifted as a whole to the target wavelength with an extra TO power consumption. The TO tuning power efficiency is ∼ 40.9 mW/FSR for each switch element. Figure 4 shows the measured transmission spectra of the switch at the "000000" state. Each plot shows four spectra from four input ports to one output port. The spectra are all normalized to a test waveguide to eliminate the effect of grating couplers. The coupling loss at 1550 nm wavelength is ∼6.7 dB/facet. The grating coupling efficiency can be further improved by an optimized design [19]. It can be seen that at the "000000" state, the input to output ports are mapped as I3-O1, I4-O2, I1-O3, and I2-O4. There is a small dip at 1555.62 nm wavelength, which originates from the internal loss of the MRRs. After subtraction of the 6.2 dB splitting loss, the average on-chip insertion loss of the 4×4 switch is ∼4.0 dB. The on-chip insertion loss originates from the waveguide crossings, the 2×2 MMIs, the MRRs, and the connection waveguides. The extracted waveguide loss is ∼2.4 dB/cm. The insertion loss of the waveguide crossings is around 0.17 dB/junction, extracted by linear fitting the accumulative loss of 10, 20, and 30 series-connected crossings. The switch insertion loss can be further reduced by optimizing the 2×2 MMIs and the waveguide crossings. The crosstalk of the switch is ∼ −20 dB at 1555.62 nm wavelength.

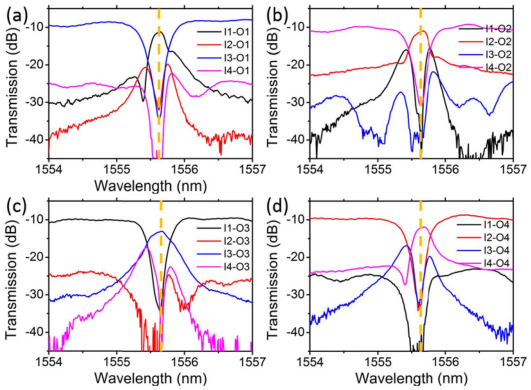

Fig. 5. Measured transmission spectra from all the four input ports to (a) O1, (b) O2, (c) O3, and (d) O4 of the switch at the "111111" state.

TABLE II
COMPARISON WITH THE REPORTED NON-BLOCKING 4×4 SWITCHES

	Power (mW)	On-chip insertion loss (dB)	Crosstalk (dB)
MRR (CROW+TO) [6]	~666[a]	3~9.7	27 (ER)[b]
MZI (FCD+TO) [7]	33.7+14.3	5.8~7.7	-17~-12
MZI (FCD) [8]	2.07~24.33	13~15	-17~-12
MZI (FCD) [12]	4.46~35.92	9~11	-19~-12
MRR (TO) [16]	10.37	NA	-13
This work (FCD +TO)	22.37+1.38	4~5.8	-20~-18.4

[a]Estimated from the given heater resistance and bias voltages. [b]ER: extinction ratio.

To switch all the DR-MZIs to the bar state, the p-i-n diode in MRR R1 of each switch element is then turned on. In this case, the 4×4 switch is reconfigured to the "111111" state. The EO tuning power consumptions are also listed in Table I. The total EO power is only 1.38 mW, which is the maximum EO tuning power among all the switching states. Figure 5 shows the measured transmission spectra of the switch at the "111111" state. At this state, the input to output ports are mapped as I1-O1, I2-O2, I3-O3, and I4-O4. The average on-chip insertion loss is increased to ∼5.8 dB due to the FCA effect. The extracted worst crosstalk at 1555.62 nm is −18.4 dB. Because of the small perturbation of refractive index upon EO tuning, the deterioration of crosstalk due to FCA is less severe than that for MZIs and MRRs. The optical 3-dB bandwidth of the switch is ∼35 GHz.

We compare the switching performances of our device with the previously reported silicon 4×4 switches, as illustrated in Table II. The device in Ref. [6] was constructed by fifth-order MRRs and based on TO effect, and hence it has a high extinction ratio of 27 dB. However, the power consumption was very large. Comparing with the other FCD-based switches, our switch shows the lowest crosstalk and on-chip insertion loss.

IV. CONCLUSIONS

In conclusion, we have experimentally demonstrated a silicon EO 4×4 non-blocking switch in a Benes fabric with DR-MZIs as switch elements. The switch footprint is 3.4 × 1.6 mm^2. Both silicon resistive microheaters and p-i-n diodes are integrated in each MRR of all the DR-MZIs for phase-error correction and fast EO switching, respectively. The minimum total TO power consumption to align all the resonances is 22.37 mW, and the maximum EO switching power is 1.38 mW. Experimental results show that the average on-chip insertion loss is in the range of 4.0 dB to 5.8 dB. The switch has an optical 3-dB bandwidth of ∼35 GHz and a crosstalk of better than −18.4 dB at the operational wavelength of 1555.62 nm. Compared with other reported 4×4 non-blocking EO switches, our device possesses the lowest crosstalk and on-chip insertion loss. With its high performances of the DR-MZI based 4×4 switch, we believe it is a promising solution for future green optical switching networks.

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REFERENCES

[1] S. J. B. Yoo, "Optical packet and burst switching technologies for the future photonic Internet," *J. Lightw. Technol.*, vol. 24, no. 12, pp. 4468–4492, Dec. 2006.
[2] A. Shacham, K. Bergman, and L. P. Carloni, "Photonic networks-on-chip for future generations of chip multiprocessors," *IEEE Trans. Comput.*, vol. 57, no. 9, pp. 1246–1260, Sep. 2008.
[3] R. G. Beausoleil, M. McLaren, and N. P. Jouppi, "Photonic architectures for high-performance data centers," *IEEE J. Sel. Topics Quantum Electron.*, vol. 19, no. 2, Mar./Apr. 2013, Art. ID 3700109.
[4] T. J. Seok, N. Quack, S. Han, and M. C. Wu, "50×50 digital silicon photonic switches with MEMS-actuated adiabatic couplers," in *Proc. Opt. Fiber Commun. Conf. (OFC)*, Mar. 2015, p. M2B.4.
[5] A. W. Poon, X. Luo, F. Xu, and H. Chen, "Cascaded microresonator-based matrix switch for silicon on-chip optical interconnection," *Proc. IEEE*, vol. 97, no. 7, pp. 1216–1238, Jul. 2009.
[6] P. DasMahapatra, A. Rohit, R. Stabile, and K. A. Williams, "Optical routing in a 4×4 matrix of fifth-order ring resonator switches," in *Proc. OptoElectron. Commun. Conf. Int. Conf. Photon. Switching*, vol. 4. Jun. 2013, p. ThM1_4.
[7] L. Lu, L. Zhou, Z. Li, X. Li, and J. Chen, "Broadband 4×4 nonblocking silicon electrooptic switches based on Mach–Zehnder interferometers," *IEEE Photon. J.*, vol. 7, no. 1, Feb. 2015, Art. ID 7800108.
[8] J. Xing *et al.*, "Nonblocking 4×4 silicon electro-optic switch matrix with low power consumption," *IEEE Photon. Technol. Lett.*, vol. 27, no. 13, pp. 1434–1436, Jul. 1, 2015.
[9] L. Chen and Y.-K. Chen, "Compact, low-loss and low-power 8×8 broadband silicon optical switch," *Opt. Exp.*, vol. 20, no. 17, pp. 18977–18985, Aug. 2012.
[10] K. Suzuki *et al.*, "Ultra-compact 8×8 strictly-non-blocking Si-wire PILOSS switch," *Opt. Exp.*, vol. 22, no. 4, pp. 3887–3894, Feb. 2014.
[11] K. Tanizawa *et al.*, "32×32 strictly non-blocking Si-wire optical switch on ultra-small die of 11×25 mm^2," in *Proc. Opt. Fiber Commun. Conf. (OFC)*, Mar. 2015, p. M2B.5.
[12] J. Xing, Z. Li, P. Zhou, X. Xiao, J. Yu, and Y. Yu, "Nonblocking 4×4 silicon electro-optic switch matrix with push–pull drive," *Opt. Lett.*, vol. 38, no. 19, pp. 3926–3929, Oct. 2013.
[13] B. G. Lee *et al.*, "Monolithic silicon integration of scaled photonic switch fabrics, CMOS logic, and device driver circuits," *J. Lightw. Technol.*, vol. 32, no. 4, pp. 743–751, Feb. 15, 2014.
[14] J. Xing, Z. Li, Y. Yu, and J. Yu, "Low cross-talk 2×2 silicon electro-optic switch matrix with a double-gate configuration," *Opt. Lett.*, vol. 38, no. 22, pp. 4774–4776, Nov. 2013.
[15] N. Sherwood-Droz *et al.*, "Optical 4×4 hitless silicon router for optical Networks-on-Chip (NoC)," *Opt. Exp.*, vol. 16, no. 20, pp. 15915–15922, Sep. 2008.
[16] R. Ji *et al.*, "Microring-resonator-based four-port optical router for photonic networks-on-chip," *Opt. Exp.*, vol. 19, no. 20, pp. 18945–18955, Sep. 2011.
[17] A. Biberman *et al.*, "Broadband silicon photonic electrooptic switch for photonic interconnection networks," *IEEE Photon. Technol. Lett.*, vol. 23, no. 8, pp. 504–506, Apr. 15, 2011.
[18] L. Lu, L. Zhou, X. Li, and J. Chen, "Low-power 2×2 silicon electro-optic switches based on double-ring assisted Mach–Zehnder interferometers," *Opt. Lett.*, vol. 39, no. 6, pp. 1633–1636, Mar. 2014.
[19] L. He *et al.*, "A high-efficiency nonuniform grating coupler realized with 248-nm optical lithography," *IEEE Photon. Technol. Lett.*, vol. 25, no. 14, pp. 1358–1361, Jul. 15, 2013.