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Continuously tunable ultra-thin silicon waveguide optical delay line

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As light cannot be stopped or directly stored in any media, optical delay lines are usually used to temporally trap the optical signals. We report a wide-range continuously tunable optical delay line chip consisting of a ring resonator array and a Mach–Zehnder interferometer (MZI) switch array on the 60-nm-thick silicon waveguide platform. The ring delay line provides continuous delay tuning of more than 10 ps with a push–pull differential tuning method. The MZI switchable delay line provides digitally programmable delay tuning with a resolution of 10 ps upon reconfiguration of the MZI switches to establish different optical routing paths. Dual-stage MZI switches are used to ensure low crosstalk with an improved signal-to-noise ratio. The delay line chip can generate a maximum delay of >1 ns with an on-chip insertion loss of 12.4 dB. Optical pulse time-division multiplexing and quasi-arbitrary waveform generation are realized based on the delay line chip. These results represent a significant step towards the realization of highly reconfigurable optical signal processors enabled by optical delay manipulation with broad applications for optical communications and microwave photonics.

OCIS codes: (130.3120) Integrated optics devices; (230.5750) Resonators; (130.4815) Optical switching devices; (070.1170) Analog optical signal processing.

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1. INTRODUCTION

Optical delay lines have multiple applications in photonic switching and signal processing [1–3]. In all optically switched telecommunication network nodes, they perform exclusive functions, such as optical packet synchronization, buffering, contention management, etc., which can greatly reduce system complexity and power consumption by removing wavelength-sensitive and hence complicated optical-to-electronic and electronic-to-optical conversion. In microwave photonics systems, they are often called true-time delay lines (TTDLs) and provide a unique solution for broadband signal processing, such as tunable high-resolution microwave filters [4,5], beam forming in phased array antennas [6,7], and so on.

Generally, there are two approaches to realize optical delays. One is slowing down light group velocity in optical waveguide structures, such as photonic crystal waveguides (PhCWs) [8–10], Bragg gratings [11,12], and resonators [13–15], as well as devices with nonlinear effects, such as stimulated Brillouin scattering [16,17] and stimulated Raman scattering [18]. Among them, the ring resonators have the advantages of a simple structure, compact size, and agile functionalities [19,20]. A variable group delay can be achieved by shifting the resonance wavelengths. For a single-ring resonator, there is an intrinsic compromise between the maximum delay and the optical bandwidth. A large delay can only be obtained with the sacrifice of its operation bandwidth. Besides, the group-velocity dispersion (GVD) around the resonance also becomes large [21]. In order to get a large delay without sacrificing the bandwidth, cascaded ring resonators have been demonstrated, including coupled-resonator optical waveguides (CROWs) [22,23] and side-coupled integrated spaced sequences of resonators (SCISSORs) [24–27]. In our previous work, we have realized continuous delay tuning of approximately 100 ps by using a reflective SCISSOR structure [28]. The other approach to generate time delays is to physically change the optical path length in serial or parallel switchable delay line structures, where the optical delay is varied by selecting different routing paths using 2×2 or $N \times N$ optical switches, respectively [29,30]. Such types of TTDLs have been demonstrated based on discrete fiber components and photonic integrated circuits [31]. As the fiber systems have poor stability and need rigorous control of fiber length, integrated TTDLs have attracted more research interest in the past decades [32–36].

Both of these two approaches have their advantages and shortcomings. The resonant delay line can realize continuous delay variation, but its delay capacity is limited by the delay-bandwidth product. The switchable delay line, on the other hand, can offer a large delay, but its resolution is limited by the tuning step. Such shortages can be overcome by combining them [37]. Compact structures can be obtained via silicon photonics integration.

In such structures, the loss has become a primary limiting factor for real-system applications, where a large delay is usually desired. As is known, the silicon waveguide loss mainly comes from the waveguide's sidewall-roughness-induced scattering loss. We recently proposed and demonstrated 60-nm-thick silicon waveguides that are less sensitive to sidewall roughness. The propagation loss can be reduced by around 5 times compared with the regular 220-nm-thick silicon strip waveguides fabricated with the same technique [38]. The silicon layer can be thinned down using thermal oxidation or plasma dry etching in a CMOS-compatible process. As the waveguide mode is less confined in the silicon core, the nonlinear effect in silicon can also be alleviated, making it possible to transmit high optical powers in the waveguide with less two-photon absorption (TPA) and the consequent free-carrier absorption (FCA).

In this work, we experimentally demonstrate a long-range continuously tunable optical delay line composed of a dual-ring slow-light section followed by a switchable delay line section. The optical delay line is built on an ultra-thin silicon waveguide platform. The experimental results show that the delay can be continuously tuned up to 1.28 ns with a maximum on-chip insertion loss of 12.4 dB. It should be noted that the loss includes the splitting loss of optical power taps which are inserted for convenient testing of the constituent components. Lower on-chip insertion losses can be expected if they are removed. The delay line chip exhibits a unique performance combination of tuning range, reconfigurability, resolution, and loss that is difficult to match with any existing delay line technology. In addition to optical delay, the chip can also provide other functionalities, including optical time-division multiplexing (OTDM) and quasi-arbitrary waveform generation (QAWG). They are implemented by setting the switch power splitting ratio and waveguide attenuation to the proper values.

2. DEVICE STRUCTURE AND FABRICATION

Figure 1(a) shows a schematic drawing of the topological structure of the entire optical delay line. The front dual-ring slow-light section allows for the continuous fine-tuning of the delay using a differential resonance shift method. We define the maximum delay tuning range of the ring section as t_{ring}, which is dependent on the ring-waveguide coupling coefficient. The followed switchable delay line comprises seven binary-delay stages enabled by eight MZI switches, allowing for the discrete coarse-tuning of the delay. The length differences of the connection waveguides between the successive switches are carefully designed so that the nth stage provides an incremental delay of $2^{(n-1)}\Delta t$, where Δt is the time delay of the first stage. When the longest path is selected, a maximum delay of $127\Delta t$ is obtained. Two types of switches are explored in our design: one based on a single MZI and the other based on dual-stage cascaded MZIs. We set $t_{\text{ring}} > \Delta t$ to ensure the minimum tuning step from the switchable delay line can be covered by the ring delay line so that the tuning is continous over the entire delay range. A variable optical attenuator (VOA) is inserted into each connection waveguide to eliminate the spurious leaked optical wave to improve the signal-to-noise ratio of the delayed optical signals [33]. Hence, this delay line structure provides unprecedented control over the delay tuning range, resolution, and crosstalk.

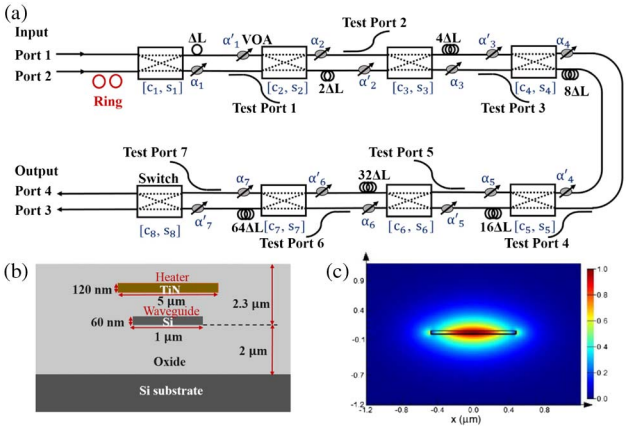

Fig. 1. (a) Architecture of the continuously tunable optical delay line structure. (b) Cross-sectional structure of the ultra-thin waveguide with a TiN heater on top. (c) Simulated x-component of the electronic field distribution for the fundamental TE mode.

Figure 1(b) shows the cross section of the thermo-optic phase shifter. Figure 1(c) shows the simulated mode profile of a 1 μm (width) × 60 nm (height) silicon waveguide for the transverse electric (TE) polarization using Lumerical MODE Solutions. It should be noted that such a thin waveguide only supports the TE mode with a low propagation loss of 0.61 dB/cm and a bending loss of approximately 0.015 dB/180° at a bending radius of 30 μm, according to our prevous work [38]. Comparing to the shallow-ridge silicon waveguide [39], the thin waveguide has a smaller bending radius, leading to a more compact photonic circuit, although the propagation loss is higher. We choose the thin silicon waveguide due to its good compromise in compactness, propagation loss, and detrimental nonlinear effect. The effective refractive index is $n_{\text{eff}} = 1.80$ at a 1.55 μm wavelength, much lower than the effective index of 2.45 for a regular 500 nm (width) × 220 nm (height) strip silicon waveguide. In our design, we taper the waveguide width to 2.5 μm for all long straight waveguides to further reduce the waveguide loss. The extracted average waveguide propagation loss is around 0.35 dB/cm. Such an improvement in the waveguide loss will lead to a delay line technology with all-optimized properties that is essential in modern microwave photonics systems and applications.

The layout of the optical delay line is illustrated in Fig. 2(a). The input, output, and test ports are all routed to the chip edge and terminated with grating couplers with a pitch of 127 μm to facilitate coupling with a fiber array. The TiN-based thin-film heaters are connected with aluminum wires to electrical pads positioned along the chip edges. The optical delay line chip was fabricated on a silicon-on-insulator (SOI) wafer with a top silicon layer thickness of 220 nm and a buried oxide layer thickness of 2 μm, using CMOS-compatible fabrication processes. The top silicon layer was first thinned down to 60 nm by thermal oxidation and HF solution wet etching. Then, the waveguides were patterned by deep ultraviolet (DUV) photolithography and transferred to the silicon layer by plasma dry etching. A 1.5-μm-thick silicon dioxide layer was deposited using chemical vapor deposition (CVD) on top of the waveguides as the upper cladding. Next, a 120-nm-thick TiN layer was sputtered and patterned to form micro-heaters. Subsequently, another 0.73-μm-thick silicon dioxide layer was deposited. Finally, contact holes were etched, and aluminum metal connections were formed by sputtering and plasma dry etching. Figure 2(b) shows the microscope image of the fabricated chip. The chip size is

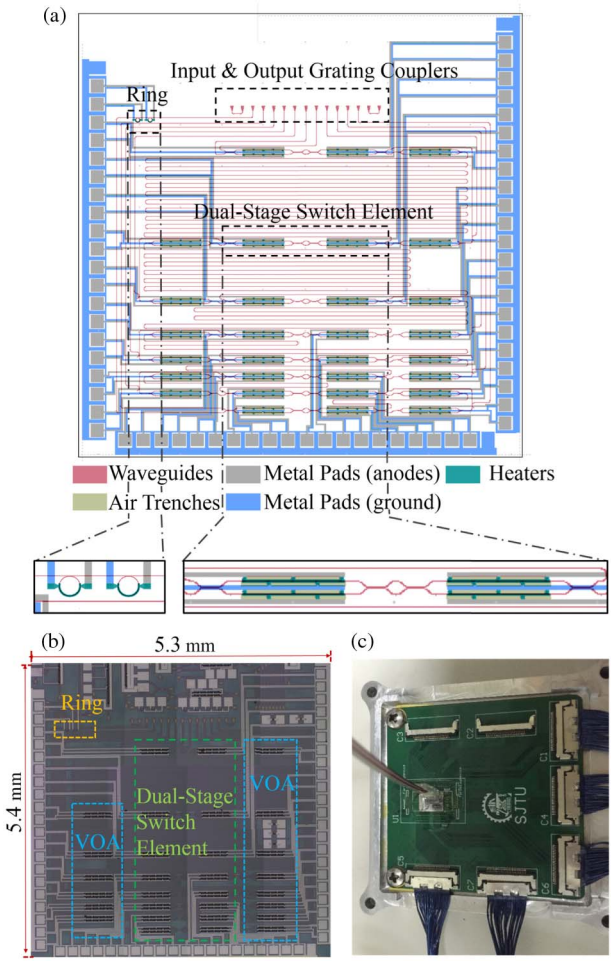

Fig. 2. (a) Overview of the continuously tunable optical delay line layout. Waveguides, heaters for thermal tuning, and metal pads for electrical connections are visible. The insets provide a closer view of the ring resonators and the dual-stage switch element. (b) Optical microscope image of the fabricated chip. (c) Photo of the packaged chip with fiber array coupling and electrical wire bonding to a PCB.

5.4 mm × 5.3 mm. A commercial fiber array is coupled and attached to the chip by using an index-matched UV adhesive. All the electrical pads are wire bonded to a printed circuit board (PCB) so that control voltages can be applied onto the chip. Figure 2(c) shows the packaged chip.

3. COMPARISON OF SINGLE AND DUAL-STAGE MZI SWITCHES

We designed two types of switches based on a single MZI and dual-stage MZIs. The dual-stage switch has identical design parameters as the single switch, as shown in Fig. 3(a). Because of the uneven splitting ratio of the multimode interferometers (MMIs) in the MZI and the unbalanced arm loss due to fabrication uncertainties, the single MZI switch has a limited switching extinction ratio (ER), as shown in Fig. 3(b). In contrast, the dual-stage MZI switch has an improved ER of more than 25 dB in the wavelength range of 1520–1580 nm. Table 1 lists the power consumption of the dual-stage MZI switch in the switchable delay line section. Ideally, the initial state of the dual-stage switch should be at the bar state. However, because of fabrication-induced random phase

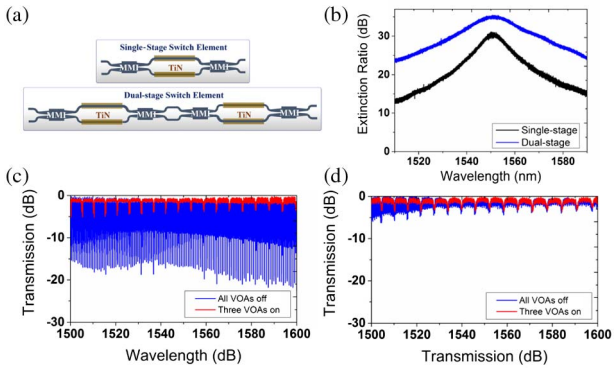

Fig. 3. (a) Structures of the single- and dual-stage MZI switch elements. (b) Extinction ratio of the single- and dual-stage MZI switch elements. Transmission spectra of the switchable delay line based on (c) the single-stage and (d) the dual-stage MZI switches.

Table 1. Power Consumption of the Dual-Stage MZI Switches

Switch #	1	2	3	4
P_{bar}/mW	1.8	0.6	1.0	13.5
P_{cross}/mW	12.5	12.7	13.0	1.2
Switch #	**5**	**6**	**7**	**8**
P_{bar}/mW	0.0	12.6	9.6	0.4
P_{cross}/mW	10.1	2.6	2.6	10.4

errors, thermal tuning with variable power consumption is required to reach the initial bar state.

As the switch has a limited ER, it causes optical leakage to the other optical path, leading to crosstalk [40]. The crosstalk can accumulate to a significant level after several stages and may severely deteriorate the transmitted signal. This eventually reduces the signal-to-noise ratio, resulting in a higher bit error rate for the delayed optical signal. The blue curve in Fig. 3(c) shows the transmission spectrum when the longest optical path is selected. A large fluctuation of >15 dB in optical power is observed, which originates from the interference among the multiple optical paths. In fact, the resonance spectrum is completely overwhelmed by the interference fringe. In order to solve this problem, the VOAs in the noise paths can be turned on to attenuate the leaked optical wave. The VOA is composed of a 1 × 1 MZI with an active arm length of 625 μm. The attenuation is around 20 dB when a 2.1 V voltage is applied. The red curve in Fig. 3(c) shows a much cleaner spectrum when three VOAs in the noise paths are turned on. Periodic resonance dips can be clearly discerned in the spectrum.

In principle, if the ER of the switch is large enough, then the crosstalk can be very low, and VOAs are not necessary. The dual-stage MZI switch can effectively increase the ER. It is made of two series-connected MZIs, with each one being independently controllable. Figure 3(d) shows the transmission spectrum for the longest optical path when three VOAs are turned off and on. Compared with the single MZI switch design, the noise is greatly reduced even when the VOAs are off. This result illustrates the superiority of the dual-stage MZI switch, which exhibits impressive suppression of the crosstalk from the inter-path interference. In the following experiment, we chose a delay line chip designed with the dual-stage switch elements.

Table 2. Comparison of Various 2 × 2 Switches[a]

	ER (dB)	P_{switch} (mW)	IL (dB)	BW (nm)
TSCR (TO) [41]	30	<10	1.2	2.2
PhC switch [42]	>20	3	<1	—
MZI (TO) [43]	~17	~3	<2.9	~110
MZI (FCD+TO) [44]	>20	—	<1	~140
MZI (FCD, double-gate) [45]	~31/43	40.8/19.1	3.5/2.5	~40
CROW (2 MRRs, FCD) [46]	~9.8	17.4	<2.0	0.48
MRR (FCD) [47]	~5[b]	0.61	~7	0.45
Our work (cascaded MZIs)	>25	<13.5	<0.5	60

[a]TSCR: triangular-shaped coupled microrings; PhC: photonic crystal; FCD: free-carrier plasma dispersion; MRR: microring resonator.
[b]Data from Fig. 9(b) of Ref. [47].

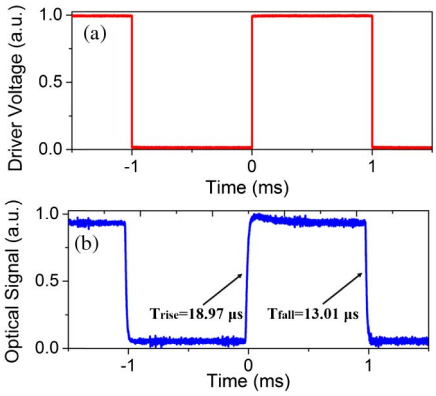

Fig. 4. Time-domain optical response of the switch element. (a) Applied square-wave electrical drive signal. (b) Measured optical waveform.

Table 2 summarizes the switching performances of the previously reported 2 × 2 switches. The insertion loss (IL) of our switch is within 0.5 dB, and the ER is larger than 25 dB. The average power consumption of the microheater for phase error correction is 1.26 mW, while the average switching power (P_{switch}) is 12.24 mW. Given its compact size, large optical bandwidth (BW) and high ER, our 2 × 2 switch based on cascaded MZIs can function as a good building block for the switchable optical delay line.

We measured the switching speed by applying a 500 Hz electrical square-wave signal onto the microheater via a radio frequency (RF) probe. The peak-to-peak drive voltage is $V_{pp} = 3.04$ V. The measured rise/fall time of the output modulated optical signal is 18.97/13.01 μs, as shown in Fig. 4.

4. OPTICAL DELAY CHARACTERIZATION

A. Ring Delay Line

We first characterized the ring resonator delay line. The input port is Port-2, and the output is Test Port-1, with the first switch configured at the bar state. The radius of the ring resonators is 25 μm, as shown in Fig. 5(a). The coupling length of the ring resonator is 3 μm, and the gap size is 0.2 μm to ensure the resonators work in the over-coupling regime to provide retardation for the optical signals. A push–pull differential tuning method was used [28]. When no voltage was applied to the ring resonators, they resonated at the wavelengths of λ_{r1} and λ_{r2} ($\lambda_{r1} < \lambda_{r2}$) because of phase errors. Then, we applied different voltages to make them red-shift to the same wavelength of λ_0 ($\lambda_0 > \lambda_{r2}$). The resonances were aligned, and the group delay reached the maximum. Next, we reduced the voltage of one ring and increased the voltage for another ring. In this way, the resonances shifted to opposite directions, with the original delay peak gradually divided into two. At the operation wavelength λ_0, the group delay continuously dropped down to 0 when the delay peaks were fully separated. It should be noted that the first-order group delay dispersion remains zero because of the symmetrical group delay profile.

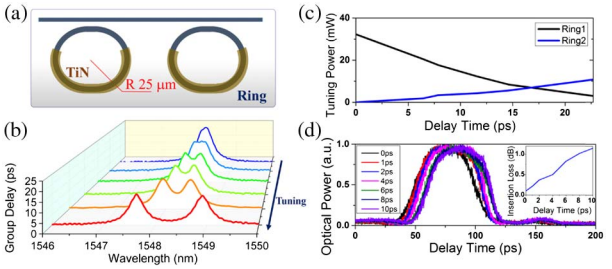

Fig. 5. (a) Dual-ring slow-light delay line structure. (b) Evolution of the ring delay spectrum upon thermal tuning. (c) Thermal tuning power of the two rings changes as a function of the delay time. (d) Optical pulse waveforms after passing through the ring delay line with various delays. The inset shows the insertion loss variation with the delay time.

Figure 5(b) shows the evolution of the ring delay spectrum upon tuning. The delay tuning range is 23 ps with a bandwidth of 60 GHz (~0.48 nm). The power consumption is 12–33 mW, as shown in Fig. 5(c). Optical pulses passing through the ring resonators with 0–10 ps delays are illustrated in Fig. 5(d). The 10 ps delay is enough to cover the tuning step of the successive switchable delay line. As the rings work in the over-coupling regime, the resonance loss for 10 ps delay is 1.1 dB.

B. Entire Delay Line

The switchable delay line following the ring resonators is composed of seven delay stages, with each one possessing a pair of waveguides with incremental differential lengths connected by a pair of switches. The length difference in the nth stage is two times longer than that in the $(n-1)$th stage. The delay tuning resolution Δt is 10 ps, given by the differential length in the first stage. Figure 6(a) shows the optical pulses after various digital delays. The operation wavelength is tuned to the off-resonance wavelength to eliminate the influence of the ring resonators. In the first seven plots, the longer waveguide in each stage is selected, and therefore, the relative delay increases exponentially from 10 to 640 ps. The shortest optical path is used as the reference path. When all the longer waveguides are selected, the delay reaches the maximum of 1.27 ns. Therefore, the delay can be increased digitally with a step of 10 ps by changing the states of the switches.

When the operation wavelength is set to the resonance wavelength λ_0 of the ring resonators, a large-range (exceeding 1.28 ns) continuous delay tuning can be achieved. To demonstrate the long-delay fine-tuning capability, we measured the optical pulses when the ring was tuned while the switchable delay was fixed at the maximum, as shown in Fig. 6(b). The optical signal quality was checked by examining the eye diagrams of a 30 Gbps $2^7 - 1$

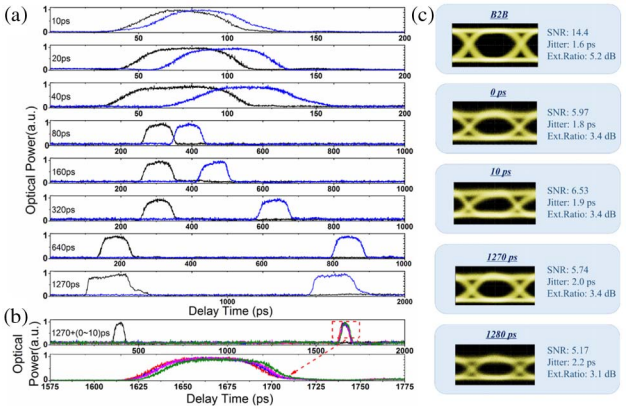

Fig. 6. (a) Optical pulse waveforms after passing through the switchable delay line. Black curves: reference pulses; blue curves: delayed pulses. (b) Optical pulse waveforms after passing through the longest optical path with delay fine tuning by the ring resonators. (c) Eye diagrams of a 30 Gbps 27^{-1} PRBS signal after various delays.

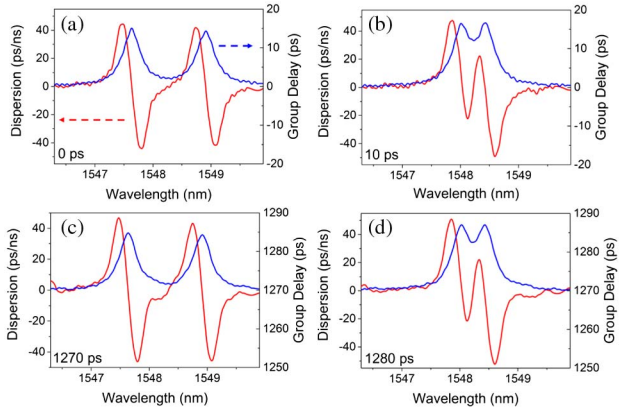

Fig. 7. Measured group delay and dispersion spectra when the entire delay line provides (a) 0 ps, (b) 10 ps, (c)1270 ps, and (d) 1280 ps delays.

pseudo-random binary sequences (PRBS) signal, as shown in Fig. 6(c). It can be seen that the signal suffers a little degradation due to the increased insertion loss for a long delay. The time jitter increases by 0.4 ps as the delay rises from 0 to 1280 ps, which is mainly attributed to the higher ASE noise incurred during optical amplification [48]. For the 30 Gbps optical signal (bit period 33.3 ps), our delay line can buffer 1280/33.3 ≈ 38 bits.

We have also measured the group delay and dispersion spectra when the delay was set to 0, 10, 1270, and 1280 ps, as illustrated in Fig. 7. The group delay spectra are similar to those in Fig. 5(b), indicating the switchable delay line has a relatively flat group delay. The group delay dispersion is hence primarily caused by the ring resonators. In the 60 GHz optical bandwidth, the group delay dispersion value is within ±25 ps/nm.

Table 3 lists the on-chip insertion loss at various delays. The reference path has an insertion loss of 8.5 dB, mainly coming from the switches (0.5 dB per switch), VOAs (0.15 dB per VOA), waveguides (1.45 dB) and coupling to Test Ports-1 to -7 (2 dB in total). The seventh stage has a 1.1 dB loss higher than the sixth stage. It can hence be deduced that the average waveguide propagation loss is ~0.35 dB/cm, lower than that of the regular 220-nm-height silicon waveguide, which is about 0.9 dB/cm, as reported in our previous work [33]. The longest path without including ring resonators has an insertion loss of 11.3 dB. An extra 1.1 dB loss is incurred when the rings are incorporated for an additional 10 ps delay. Therefore, the maximum insertion loss is 12.4 dB for the longest delay of 1.28 ns.

Table 3. On-Chip Insertion Loss of the Switchable Delay Line at Various Delays

Stage	0[a]	1	2	3	4	5	6	7	All
Delay/ps	0	10	20	40	80	160	320	640	1270
Loss/dB	8.5	8.5	8.5	8.6	8.7	9.0	9.5	10.6	11.3

[a]The shortest optical path (reference) is selected.

Table 4 compares our device with various state-of-the-art integrated optical delay lines, including 4-bit and 7-bit true-time delay lines (RTTDLs) [6,33], CROWs [49], SCISSORs [27], PhCWs [50,51], gratings [52], and MEMS-actuated delay lines [53,54]. Our device provides superior balanced optical delay performances, such as low loss, large delay tuning range, high resolution, and high tuning efficiency.

5. OTDM AND QAWG EXPERIMENT

Our delay line structure could form the basis for a host of powerful new coherent information processing technologies with powerful manipulation on pulse division and envelope tailoring. OTDM has wide applications in constructing large-capacity flexible optical networks and optical data analyses [55]. A lot of research has been reported in which the time mapping module is configured using specially designed mechanical tunable fiber stretchers. In comparison, silicon-based optical pulse multiplexing offers the intrinsic advantages of compact size and easy integration of multiple optical and electrical components.

Table 4. Comparison of Various Continuously Tunable Delay Lines

	Delay Range (ps)	Resolution (ps)	Bandwidth (nm)	Delay Loss (dB/ps)	Power Efficiency (mW/ps)	Footprint (mm^2)
4-bit RTTDL [6]	12,350	850	Large	1.9E-4	0.02	3825
7-bit RTTDL[33]	1270	10	Large	0.013	1.09	11.84
CROWs [49]	800	100	0.05	0.01	5	7
SCISSORs [27]	345	Small	>0.08	0.06	0.07	0.125
PhCWs [50]	54	Small	>3	0.17	11	0.06
PhCWs [51]	70	Small	—	—	1.143	0.007
Grating [52]	96	Small	0.8	0.001	11	0.015
MEMS [53,54]	94	Small	~0.04	0.24	—	<0.001
Our work	1280	Small	0.48	0.01	0.05	28.62

Our optical delay line can be reconfigured for OTDM applications, in which the switches are set to even splitting, offering multiple parallel channels for the incoming optical wave to travel through. When the nth stage is set to even splitting, then a dual-channel OTDM results with a time interval of $2^{n-1}\Delta t$. When all seven stages are set to even splitting, then a 2^7-channel OTDM can be realized. Such an OTDM scheme can be useful in the generation of high repetition rate pulse trains for optical sampling in photonic analog-to-digital conversion systems [56,57].

The switchable delay line can be modeled using the transfer matrix method. The transfer matrix of the ith switch is expressed as $T_i = a_i\begin{bmatrix} c_i & -s_i \\ s_i & c_i \end{bmatrix}(i = 1, 2, \ldots, 8)$, where c_i and s_i are the ideal transmission coefficients of the bar port and cross port ($c_i^2 + s_i^2 = 1$), respectively, and $a_i(a_i < 1)$ accounts for the loss of the coupler. The transfer matrix of the waveguide pairs between the ith and $(i+1)$th switches is given by $D_i = \begin{bmatrix} \alpha_i' \exp(-j2^{i-1}\omega\Delta t) & 0 \\ 0 & \alpha_i \end{bmatrix}(i = 1, 3, 5, 7)$ or $D_i = \begin{bmatrix} \alpha_i & 0 \\ 0 & \alpha_i' \exp(-j2^{i-1}\omega\Delta t) \end{bmatrix}(i = 2, 4, 6)$, where ω is the optical wave angular frequency, and α_i and α_i' are the transmission coefficients of the shorter and longer waveguides, respectively. The magnitudes of α_i and α_i' can be varied by the VOA integrated in the corresponding delay waveguide. The transfer matrix of the switchable delay line can thus be expressed as

$$H = T_8\left(\prod_{i=7}^{1} D_i T_i\right). \tag{1}$$

If the input is Port-1 and output is Port-3, then the transfer function that links the input to output is given by $H_{11}(\omega)$.

In our proof-of-concept experiment, we chose $c_i^2 = 0.5$ $(i = n, n+1)$ and $c_i = 0$ $(i \neq n, n+1)$ to realize the dual-channel OTDM. Initially, the transmission coefficients satisfy $\alpha_i' < \alpha_i \times (i = 1, 2, \ldots, 7)$, due to the higher loss of the longer waveguide. In order to balance the optical power of the two output OTDM pulses, the attenuation in the shorter waveguide was increased by turning on the VOA so that both waveguides have the equal transmission of α_n'.

The output optical signal $s_{\text{out}}(t)$ can be expressed as the convolution of the input signal $s_{\text{in}}(t)$ and the delay chip temporal impulse response $h_{11}(t)$:

$$s_{\text{out}}(t) = s_{\text{in}}(t) * \sum_{i=1}^{2} A\delta[t - (i-1)2^{n-1}\Delta t]. \tag{2}$$

Here, A is the peak amplitude of the output signal, given by

$$A = A_{\text{ref}}\frac{\alpha_n'}{2\alpha_n}, \tag{3}$$

$$A_{\text{ref}} = \prod_{i=1}^{8} a_i \prod_{i=1}^{7} \alpha_i. \tag{4}$$

A_{ref} is the peak amplitude of the pulse that goes directly through the reference optical path with the VOAs off, assuming the input pulse amplitude is 1. The factor 1/2 on the right side of Eq. (3) represents the division of the pulse by the two delay branches, and α_n'/α_n represents the attenuation by the VOA. The relative optical power of the OTDM pulses is given by $|A|^2$.

Figure 8(a) shows the OTDM measurement results when only one stage is set for even splitting. The operation wavelength is tuned to an off-resonance wavelength. A dual-channel OTDM with a time interval of 10–640 ps is demonstrated. The small peak in the pulse tail is attributed to the limited bandwidth of the photodiode. The relative peak height values are listed in Table 5.

When the delay line is configured for the 2^n-channel OTDM by setting the last n stages to even splitting, then the output optical signal $s_{\text{out}}(t)$ can be expressed as

$$s_{\text{out}}(t) = s_{\text{in}}(t) * \sum_{i=1}^{2^n} A\delta[t - (i-1)2^{7-n}\Delta t]. \tag{5}$$

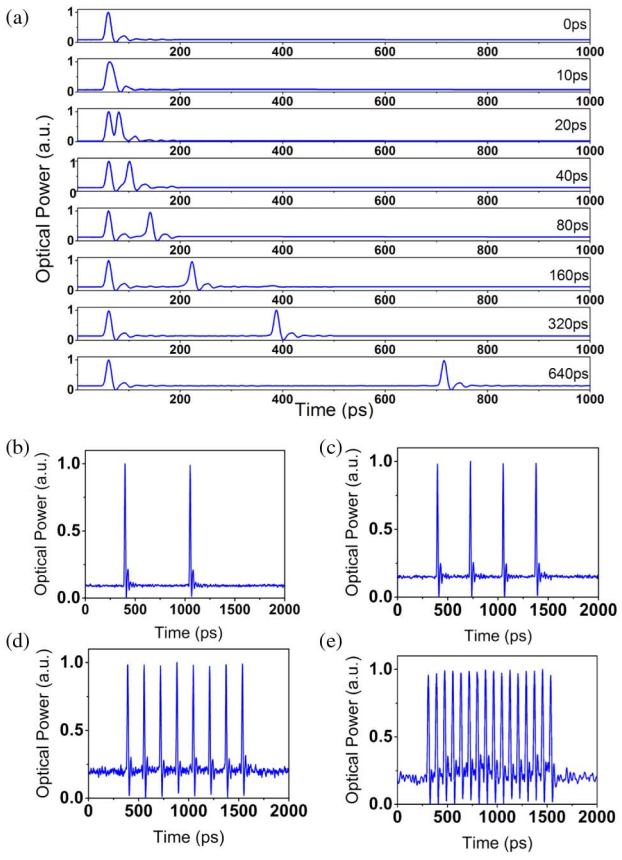

Fig. 8. (a) Dual-channel OTDM waveforms with time interval varying from 10 to 640 ps when one switchable delay line stage is in even splitting. (b)–(e) Multi-channel OTDM waveforms when the last (b) one stage, (c) two stages, (d) three stages, and (e) four stages are set to even splitting.

Table 5. Relative Peak Height in the Dual-Channel OTDM

Stage #	1	2	3	4	5	6	7
A/A_{ref}	0.50	0.50	0.49	0.49	0.47	0.45	0.40

Here, the peak height is

$$A = A_{\text{ref}} 2^{-\frac{n+1}{2}} \prod_{i=8-n}^{7} \frac{\alpha_i'}{\alpha_i}. \tag{6}$$

Figures 8(b)–8(e) present the 4-, 8-, and 16-channel OTDMs when the last 2, 3, and 4 stages are set to even splitting. The values of A/A_{ref} are 0.25, 0.17, and 0.11, respectively.

Optical arbitrary waveform generation (OAWG) can be used in wireless communications, radar, and optical computing [58]. The optical pulse shaper based on the finite impulse response (FIR) has been reported to be able to generate complex waveforms with compact sizes and electronic compatibility [59]. The integrated approach to generate programmable waveforms based on silicon platforms has also been demonstrated, where the optical delay elements accurately manipulate the individual waveform features [60]. Our delay line can also be used to generate quasi-arbitrary waveforms. In the OTDM application, the input pulse is divided into multiple pulses with equal peak powers. However, in the OAWG application, the pulse peak power needs to be varied to give an arbitrary envelope. This can be acheived by tuning the switch splitting ratio and VOA attenuation. The OTDM can be regarded as a special case for OAWG.

In our experiment, we set $c_i = 0$ $(i = 1, 2, 3, 4)$ so that light passes through the first four stages without splitting to simplify the system. The output optical signal $s_{\text{out}}(t)$ can be expressed as

$$s_{\text{out}}(t) = s_{\text{in}}(t) * \sum_{i=1}^{8} A_i \delta[t - (i-1)16\Delta t]. \tag{7}$$

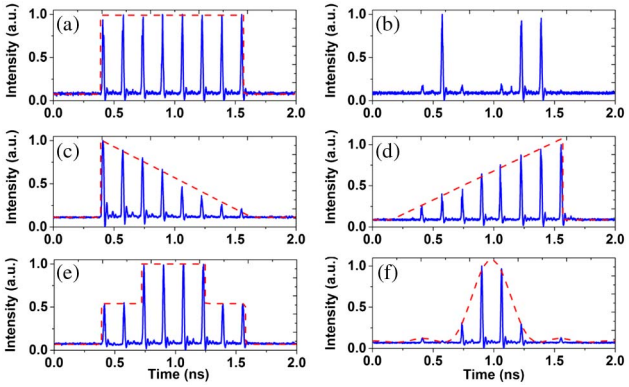

Fig. 9. Measured waveforms (blue solid line) from the QAWG: (a) square waveform, (b) chirp pulse waveform, (c) sawtooth waveform, (d) reverse sawtooth waveform, (e) staircase waveform, and (f) sinc-function waveform. The red dashed lines outline the envelopes of the ideal waveforms.

Here, A_i is given by

$$\begin{cases} A_1 = A_{\text{ref}}\rho_5\rho_6\rho_7 s_5 s_6 s_7 s_8 \\ A_2 = -A_{\text{ref}}\rho_5'\rho_6\rho_7 c_5 c_6 s_7 s_8 \\ A_3 = -A_{\text{ref}}\rho_5\rho_6'\rho_7 s_5 c_6 c_7 s_8 \\ A_4 = -A_{\text{ref}}\rho_5'\rho_6'\rho_7 c_5 s_6 c_7 s_8 \\ A_5 = -A_{\text{ref}}\rho_5\rho_6\rho_7' s_5 s_6 c_7 c_8 \\ A_6 = A_{\text{ref}}\rho_5'\rho_6\rho_7' c_5 c_6 c_7 c_8 \\ A_7 = -A_{\text{ref}}\rho_5\rho_6'\rho_7' s_5 c_6 s_7 c_8 \\ A_8 = -A_{\text{ref}}\rho_5'\rho_6'\rho_7' c_5 s_6 s_7 c_8 \end{cases}. \tag{8}$$

In the above equations, we introduce two additional parameters ρ_i and ρ_i' so that $\rho_i\alpha_i$ and $\rho_i'\alpha_i (i = 5, 6, 7)$ represent the optical field transmissions through the shorter and longer waveguides in the ith stage with the VOAs turned on, respectively. It should be noted that c_i and s_i are inter-dependent, and some variables have the same effect on A_i. For example, the variables (c_5, s_5), ρ_5, and ρ_5' control the relative power ratio between the first two branches, and thereby they should be regarded as one control variable (thus, we set $\rho_5 = 1$, $\rho_5' = \frac{\alpha_5'}{\alpha_5} = 0.94$ fixed). Similarly, the variables (c_8, s_8), ρ_7, and ρ_7' control the relative power ratio between the last two branches and should also be regarded as one variable $(\rho_7 = 1, \rho_7' = \frac{\alpha_7'}{\alpha_7} = 0.8$ fixed). Therefore, the available tuning parameters in the delay line are c_5, c_6, c_7, c_8, and ρ_6'/ρ_6. The coefficients $A_1 - A_8$ cannot be independently determined, but certain typical waveforms (such as square, chirp pulse, sawtooth, staircase, and sinc function waveforms) can still be implemented, as shown in Fig. 9. The envelope of the pulse train is normalized to units. The values of the tuning variables for each waveform are listed in Table 6. It suggests that our delay line chip can work as a QAWG. The QAWG has a wide operation bandwidth, as the frequency is determined by the time delay between the series of the switches. The envelopes of the pulses are fitted using the nonlinear least-squares method, and the relative error is less than 2%.

6. CONCLUSIONS

We have demonstrated a continuously tunable delay line combining ring resonators and a series-connected switch array. The switch array provides large-range coarse tuning of the delay, while the rings give short-range fine tuning. The dual-stage MZI switch elements are adopted to improve the switching extinction ratio. The delay line chip is implemented on a 60-nm-thick silicon waveguide platform, with an average waveguide loss of 0.35 dB/cm. The maximum delay tuning range is 1.28 ns, and the on-chip insertion loss is 12.4 dB. A 30 Gbps OOK signal was successfully transmitted through the delay line chip under various delays with a high signal fidelity.

Table 6. Typical Waveforms and the Corresponding Delay Line Setting Coefficients

Waveforms	$[A_1, A_2, A_3, A_4, A_5, A_6, A_7, A_8]/A_{\text{ref}}$	$[c_5, c_6, c_7, c_8]$	$[\rho_6, \rho_6']$
Square	[0.19, −0.19, −0.19, −0.19, −0.19, 0.19, −0.19, −0.19]	[0.73, 0.71, 0.71, 0.78]	[0.90, 0.90]
Chirp pulse	[0.00, −0.23, −0.04, 0.00, 0.00, 0.22, −0.23, 0.00]	[0.93, 1.00, 0.37, 0.95]	[0.90, 0.90]
Sawtooth	[0.27, −0.25, −0.24, −0.22, −0.18, 0.17, −0.13, −0.12]	[0.70, 0.71, 0.74, 0.61]	[1.00, 0.81]
Reverse sawtooth	[0.14, −0.15, −0.16, −0.17, −0.18, 0.20, −0.20, −0.21]	[0.75, 0.71, 0.71, 0.85]	[0.82, 0.90]
Staircase	[0.16, −0.16, −0.22, −0.22, −0.22, 0.22, −0.16, −0.16]	[0.73, 0.71, 0.81, 0.78]	[0.90, 0.90]
Sinc function	[0.12, −0.07, −0.18, −0.31, −0.30, 0.17, −0.07, −0.12]	[0.73, 0.49, 0.93, 0.78]	[0.88, 0.90]

The optical delay line chip offers a route to tailor the pulse train in a reconfigurable manner. Optical pulse multiplexing was realized based on the delay line chip where certain stages of switches were configured to give an even splitting ratio. Such an OTDM scheme can be useful in the generation of high repetition rate pulse trains for optical sampling. QAWG has also been demonstrated when the switch splitting ratio and VOA attenuation were adjusted to give unequal pulse magnitudes. The realization of OTDM and QAWG based on the delay line chip demonstrates its flexibility and reconfigurability, suggesting the chip can be potentially used as a powerful programmable optical signal processor.

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